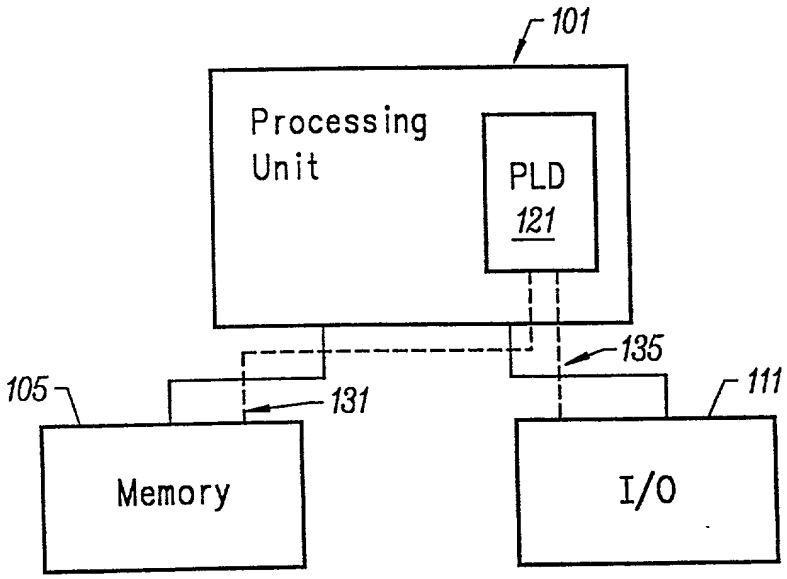

101
Processing Unit
PLD
121
135
105
131
111
Memory
I/O

FIG. 1

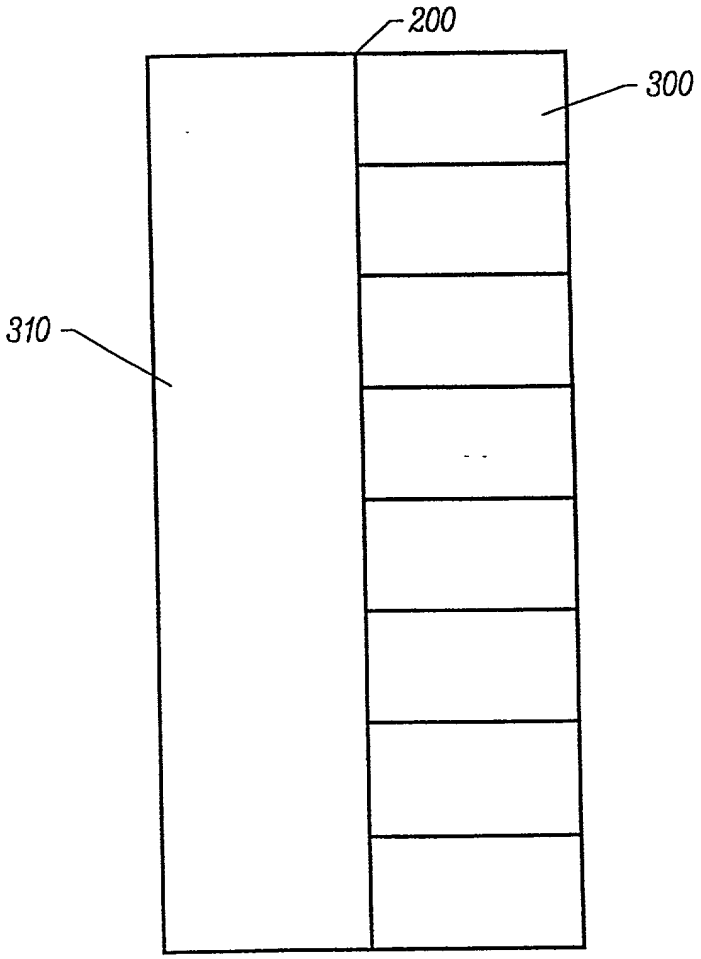

200
300
310

FIG. 3

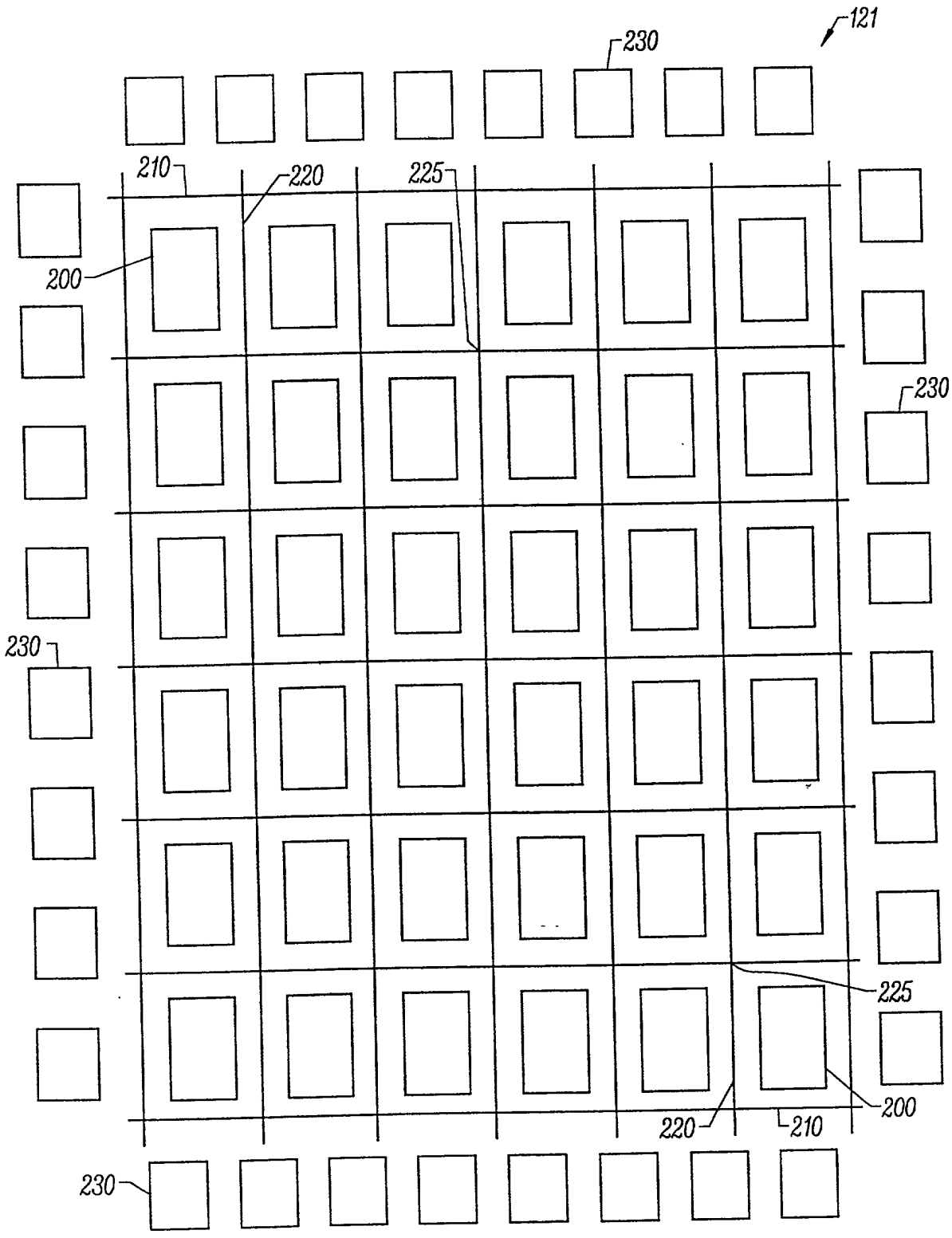


FIG. 2

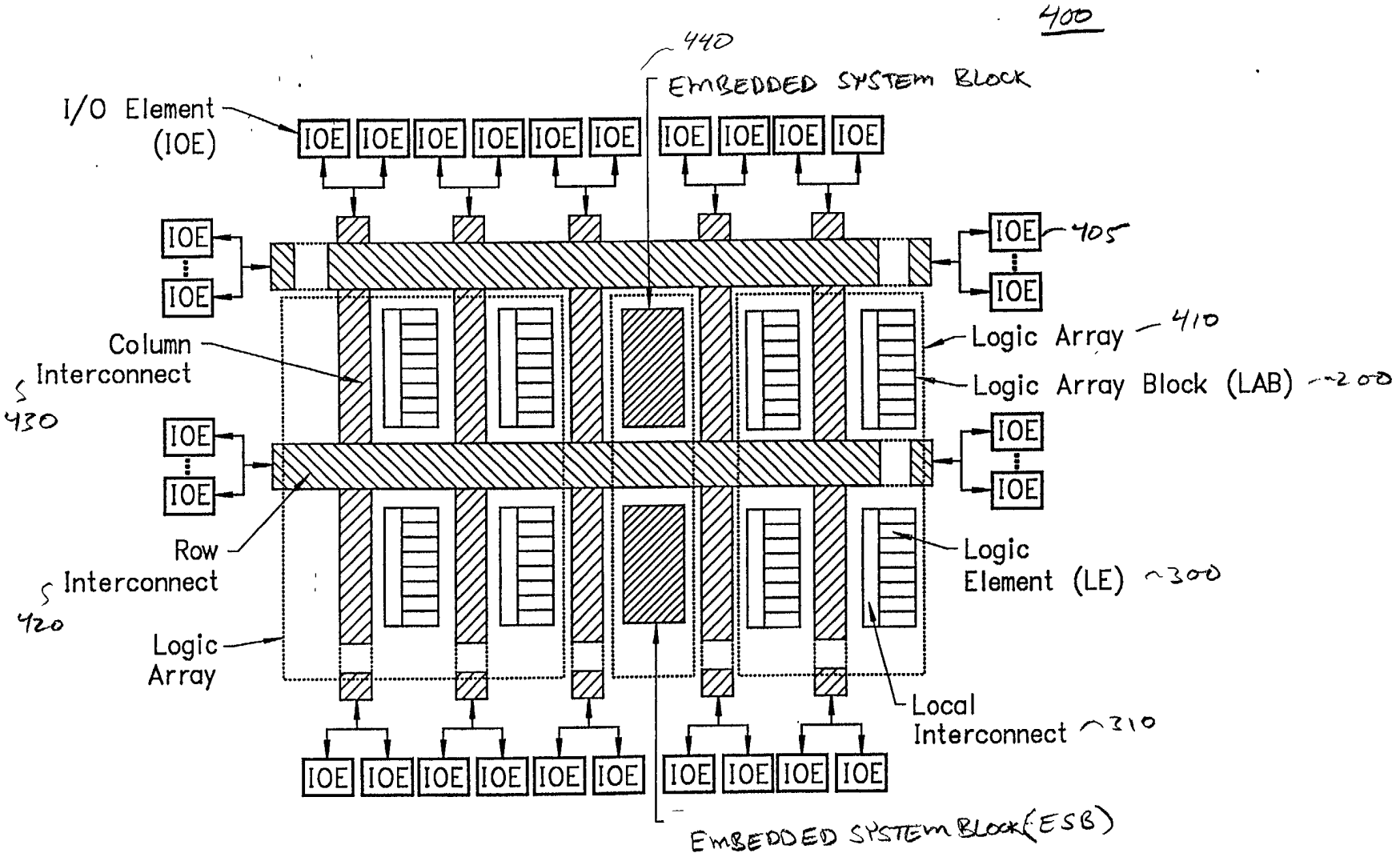


FIG. 4

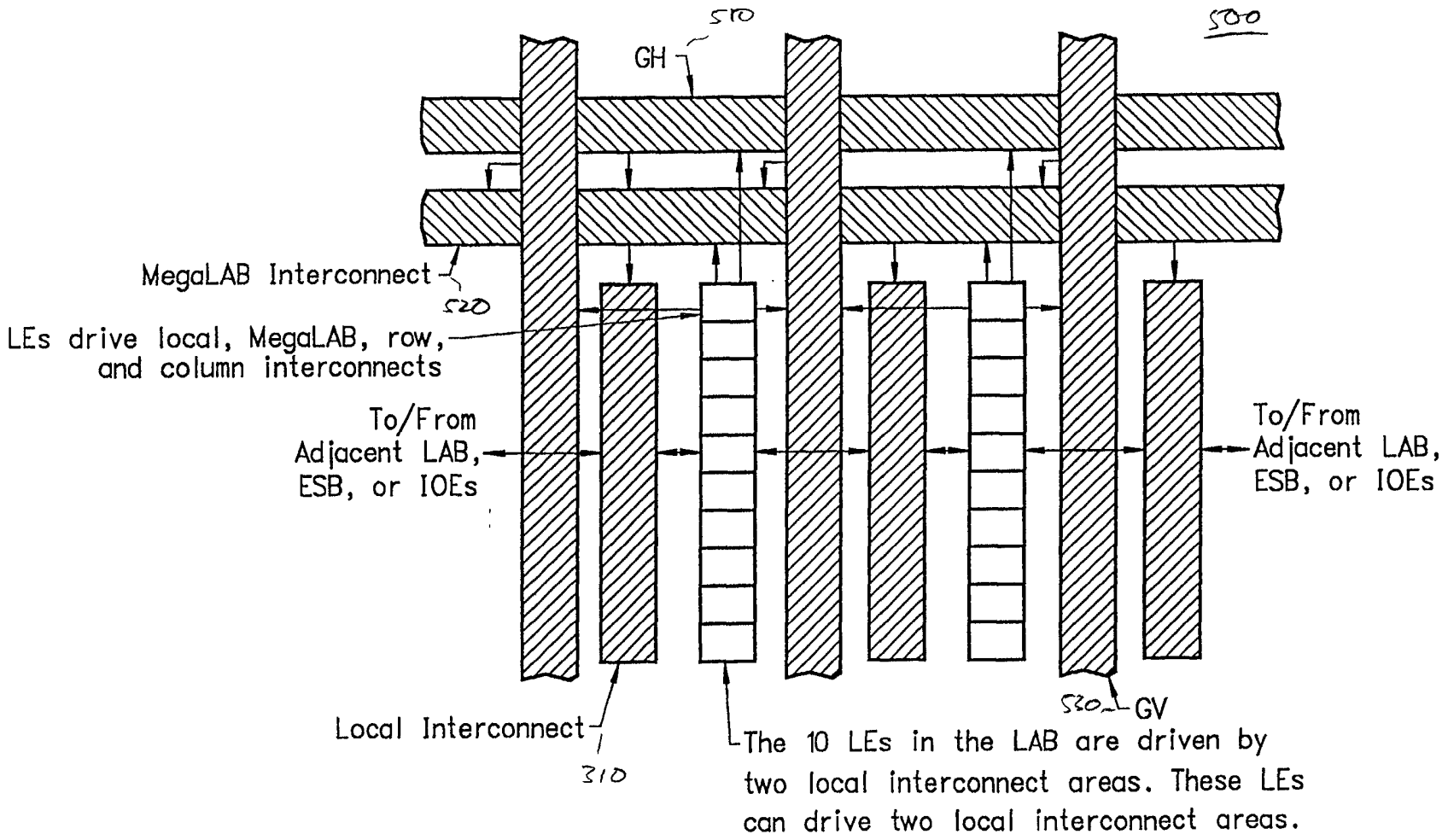


FIG. 5

600

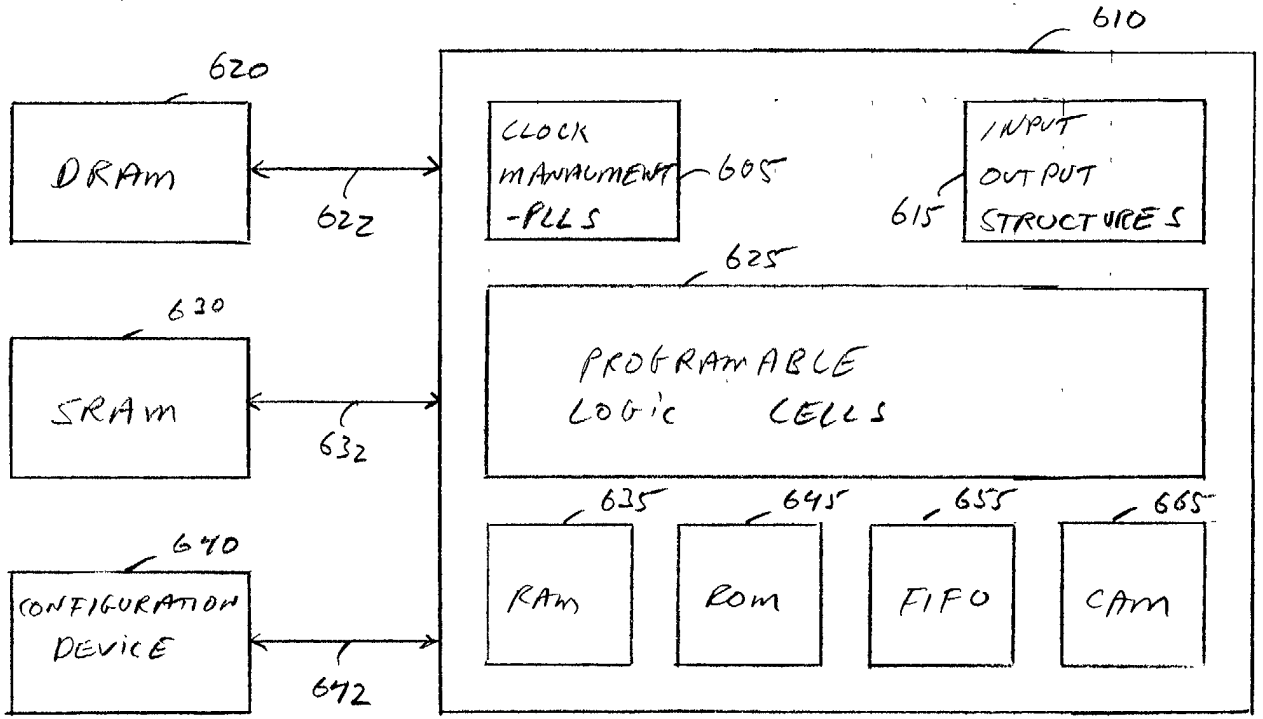

610
620
DRAM
622
630
SRAM
632
640
CONFIGURATION DEVICE
642
CLOCK MANAGEMENT -PLLS
605
615
INPUT OUTPUT STRUCTURES
625
PROGRAMABLE LOGIC CELLS
635
RAM
645
ROM
655
FIFO
665
CAM

FIGURE 6

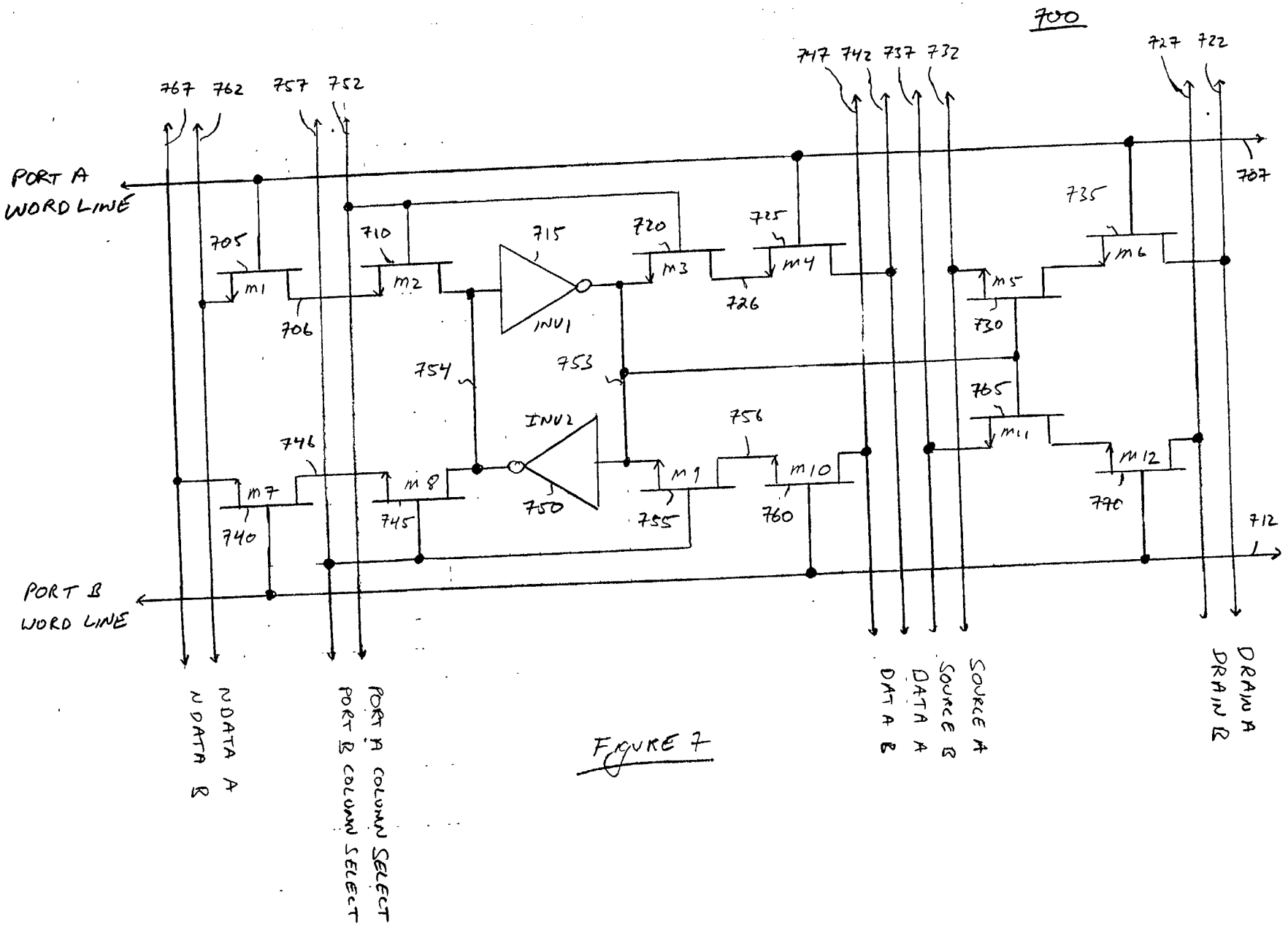

700
767
762
757
752
747
742
737
732
727
722
PORT A WORD LINE
707
705
710
715
720
725
735
m1
m2
m3
m4
m5
m6
706
726
730
INV1
754
753
INV2
765
m11
m12
746
756
m7
m8
m9
m10
740
745
750
755
760
770
712
PORT B WORD LINE
NDATA A
NDATA B
PORT A COLUMN SELECT
PORT B COLUMN SELECT
DATA A
DATA B
SOURCE A
SOURCE B
DRAIN A
DRAIN B

FIGURE 7

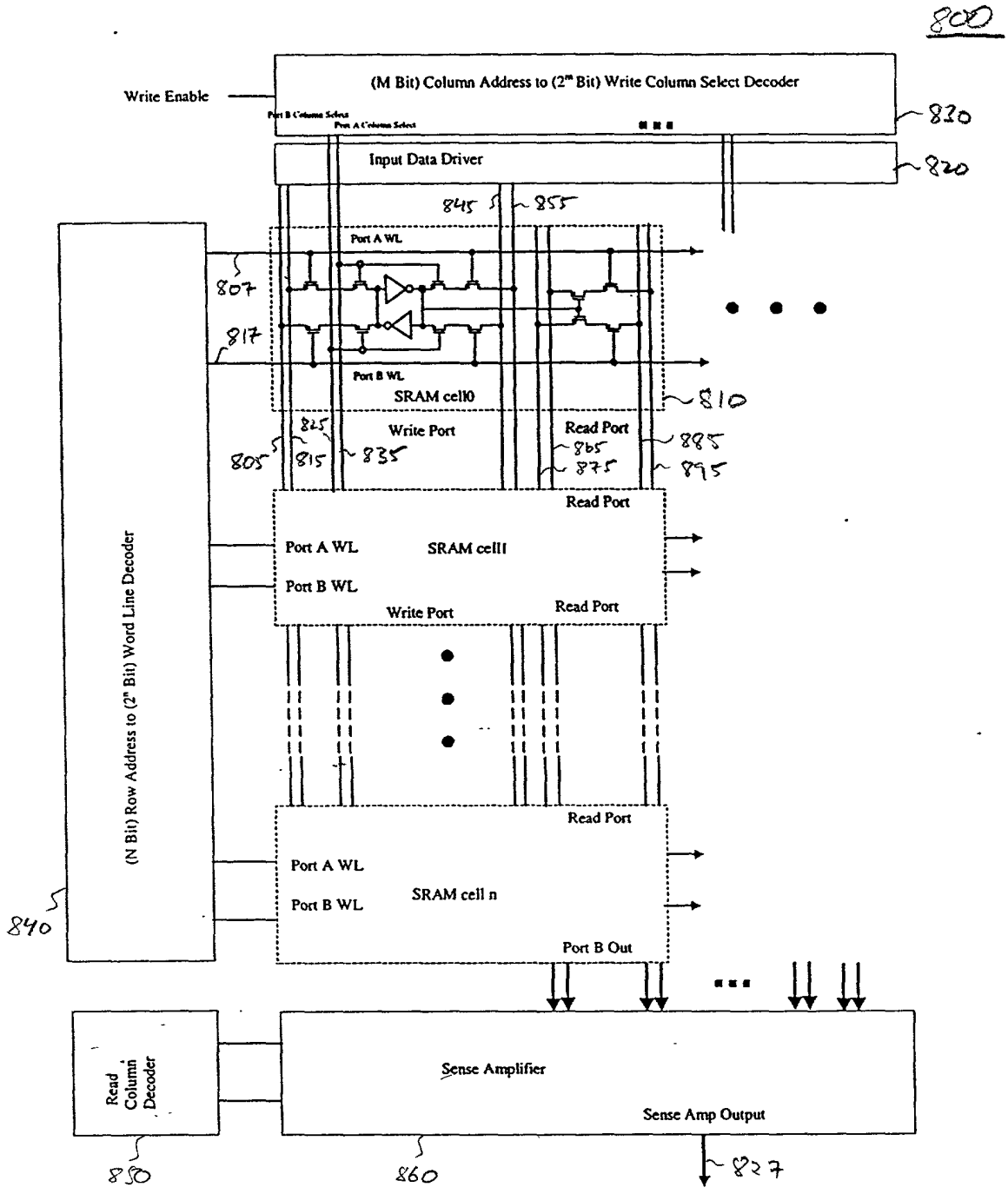

800
Write Enable
(M Bit) Column Address to (2^m Bit) Write Column Select Decoder
820
Input Data Driver
820
845
855
Port A WL
807
817
Port B WL
SRAM cell0
810
825
Write Port
Read Port
805
815
835
865
885
875
895
Read Port
Port A WL
SRAM cell1
Port B WL
Write Port
Read Port
Read Port
Port A WL
Port B WL
SRAM cell n
Port B Out
(N Bit) Row Address to (2^n Bit) Word Line Decoder
840
Read Column Decoder
Sense Amplifier
Sense Amp Output
850
860
827

FIGURE 8

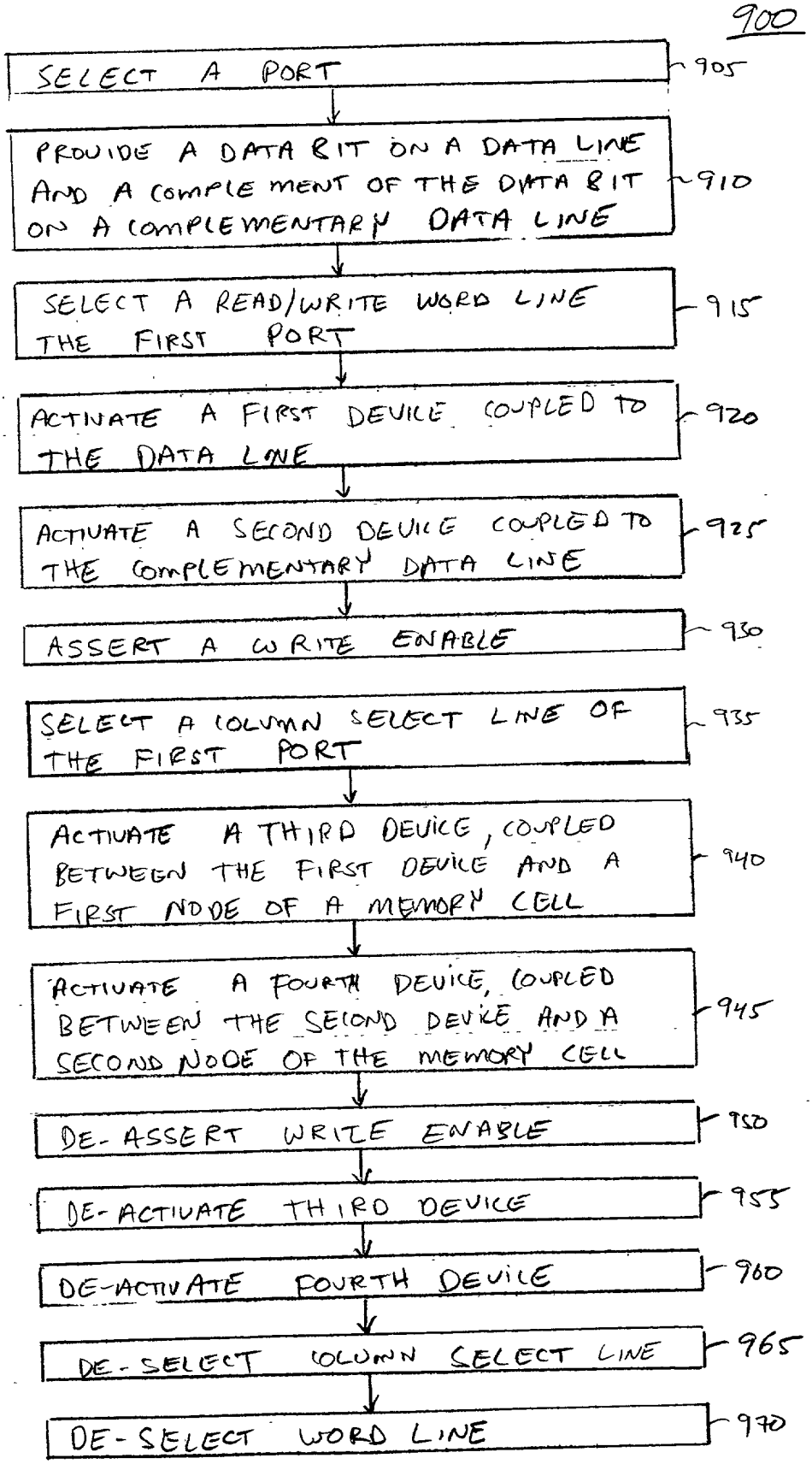

900
SELECT A PORT
905
PROVIDE A DATA BIT ON A DATA LINE AND A COMPLEMENT OF THE DATA BIT ON A COMPLEMENTARY DATA LINE
910
SELECT A READ/WRITE WORD LINE THE FIRST PORT
915
ACTIVATE A FIRST DEVICE COUPLED TO THE DATA LINE
920
ACTIVATE A SECOND DEVICE COUPLED TO THE COMPLEMENTARY DATA LINE
925
ASSERT A WRITE ENABLE
930
SELECT A COLUMN SELECT LINE OF THE FIRST PORT
935
ACTIVATE A THIRD DEVICE, COUPLED BETWEEN THE FIRST DEVICE AND A FIRST NODE OF A MEMORY CELL
940
ACTIVATE A FOURTH DEVICE, COUPLED BETWEEN THE SECOND DEVICE AND A SECOND NODE OF THE MEMORY CELL
945
DE-ASSERT WRITE ENABLE
950
DE-ACTIVATE THIRD DEVICE
955
DE-ACTIVATE FOURTH DEVICE
960
DE-SELECT COLUMN SELECT LINE
965
DE-SELECT WORD LINE
970

Figure 9

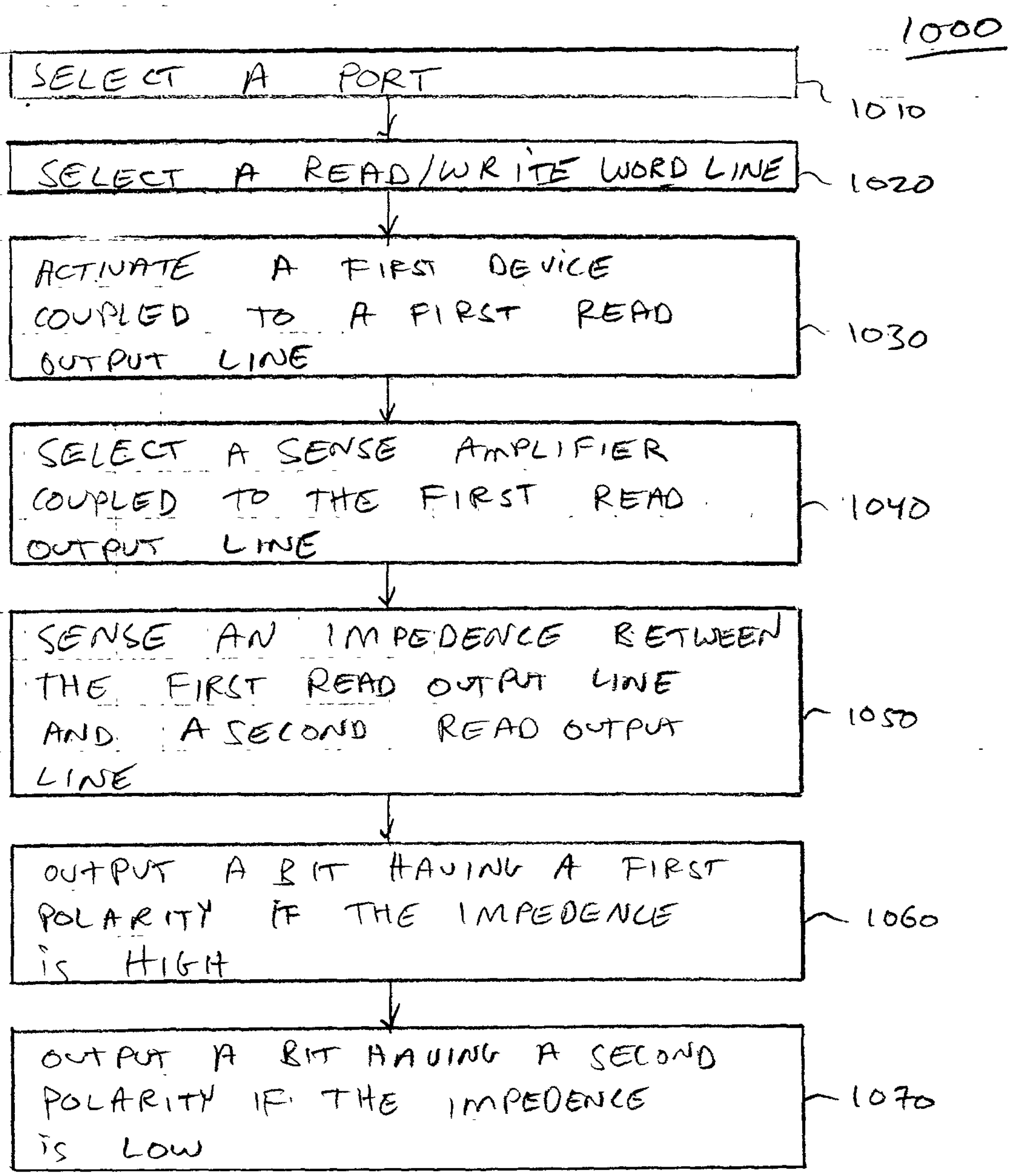

1000
SELECT A PORT
1010
SELECT A READ/WRITE WORD LINE
1020
ACTIVATE A FIRST DEVICE COUPLED TO A FIRST READ OUTPUT LINE
1030
SELECT A SENSE AMPLIFIER COUPLED TO THE FIRST READ OUTPUT LINE
1040
SENSE AN IMPEDENCE BETWEEN THE FIRST READ OUTPUT LINE AND A SECOND READ OUTPUT LINE
1050
OUTPUT A BIT HAVING A FIRST POLARITY IF THE IMPEDENCE IS HIGH
1060
OUTPUT A BIT HAVING A SECOND POLARITY IF THE IMPEDENCE IS LOW
1070

FIGURE 10

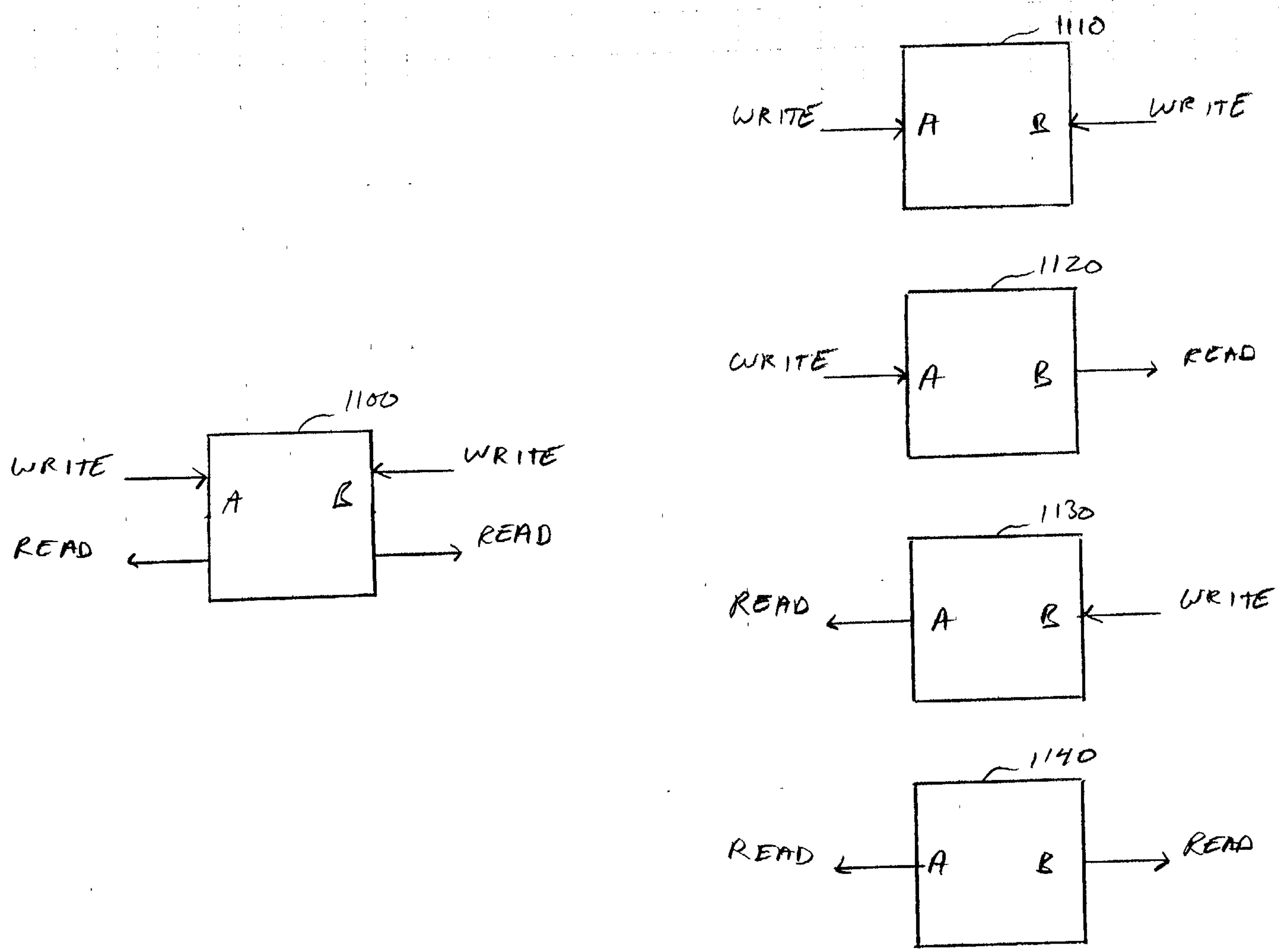

1100
WRITE
A
B
WRITE
READ
READ
1110
WRITE
A
B
WRITE
1120
WRITE
A
B
READ
1130
READ
A
B
WRITE
1140
READ
A
B
READ

FIGURE 11

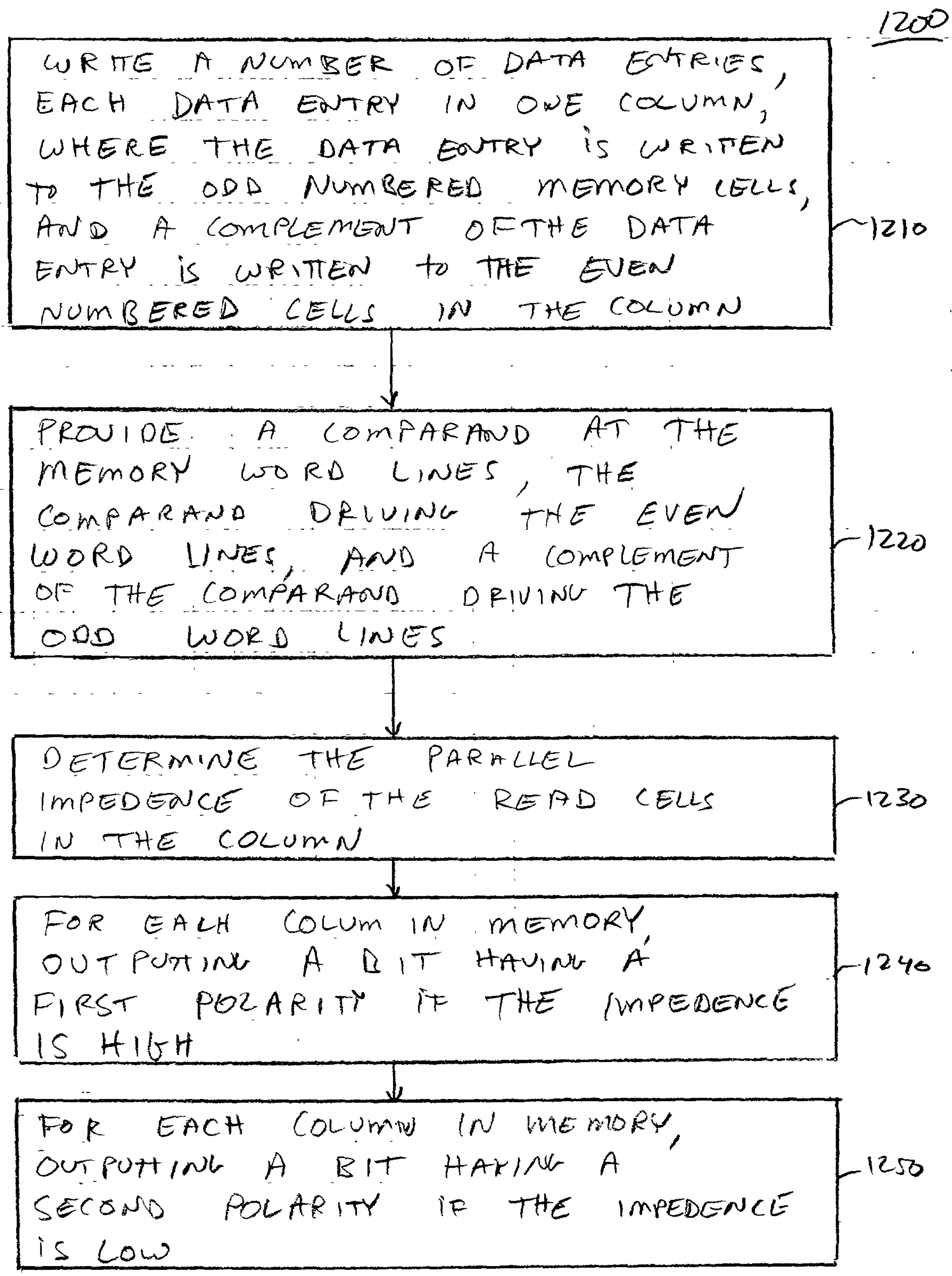

1200
WRITE A NUMBER OF DATA ENTRIES, EACH DATA ENTRY IN ONE COLUMN, WHERE THE DATA ENTRY IS WRITTEN TO THE ODD NUMBERED MEMORY CELLS, AND A COMPLEMENT OF THE DATA ENTRY IS WRITTEN TO THE EVEN NUMBERED CELLS IN THE COLUMN
1210
PROVIDE A COMPARAND AT THE MEMORY WORD LINES, THE COMPARAND DRIVING THE EVEN WORD LINES, AND A COMPLEMENT OF THE COMPARAND DRIVING THE ODD WORD LINES
1220
DETERMINE THE PARALLEL IMPEDENCE OF THE READ CELLS IN THE COLUMN
1230
FOR EACH COLUM IN MEMORY, OUTPUTTING A BIT HAVING A FIRST POLARITY IF THE IMPEDENCE IS HIGH
1240
FOR EACH COLUMN IN MEMORY, OUTPUTTING A BIT HAVING A SECOND POLARITY IF THE IMPEDENCE IS LOW
1250

Figure 12

1300

PRODUCT TERM = $A \cdot B \cdot \overline{C}$ (1305)

A "MATCH" OCCURS WHEN A = 1, B = 1, C = 0 (1310)

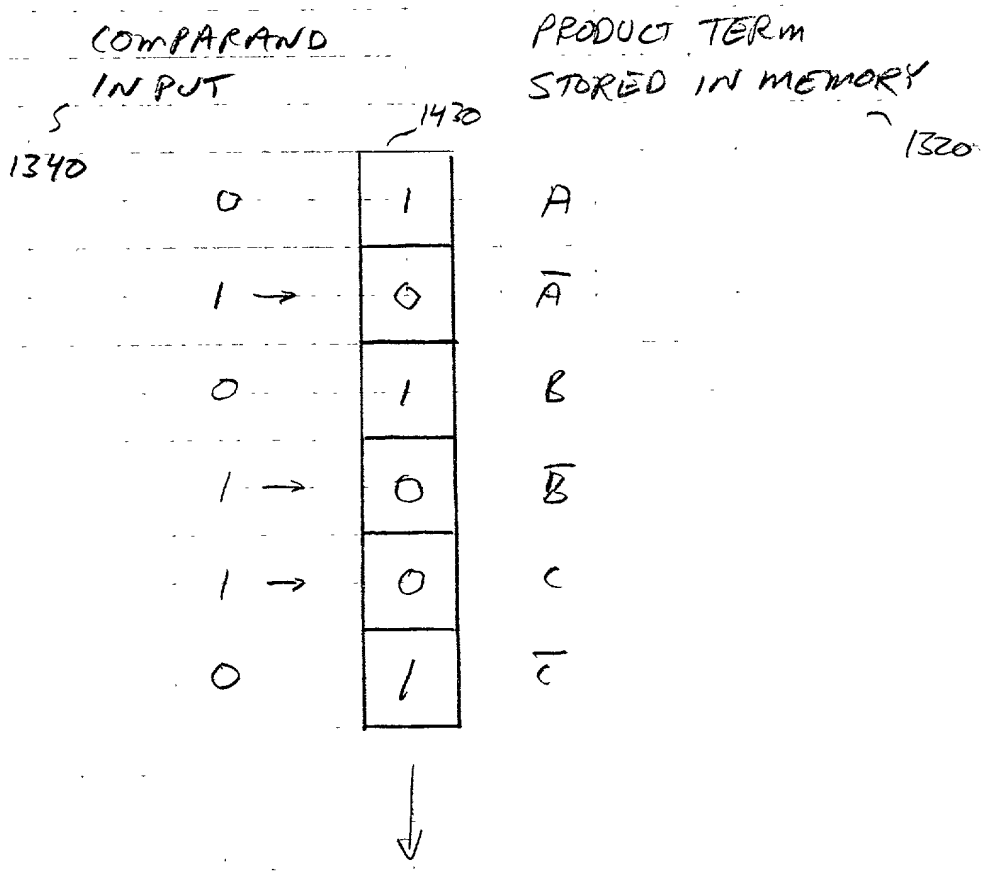


FIGURE 13

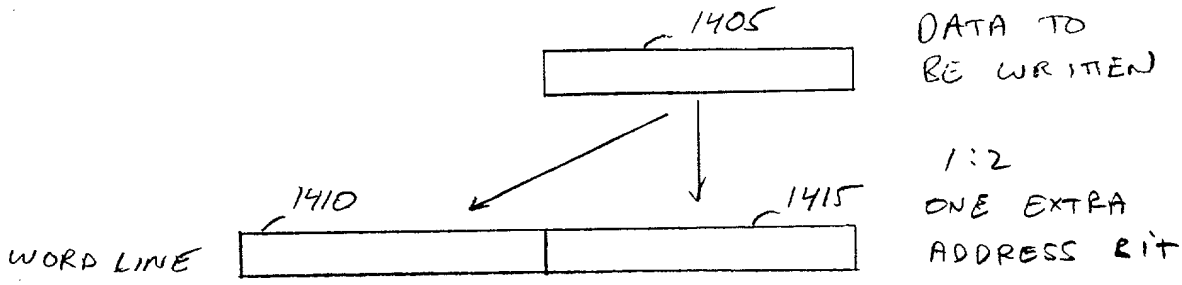


Figure 14A

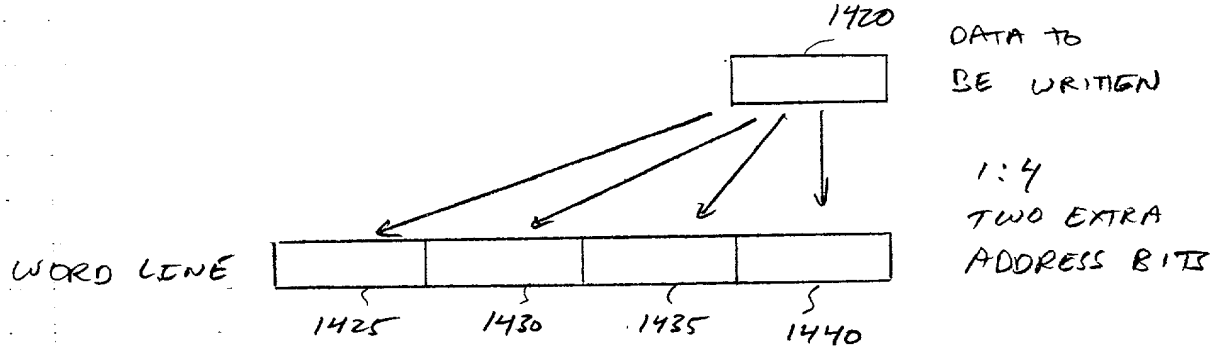


Figure 14B

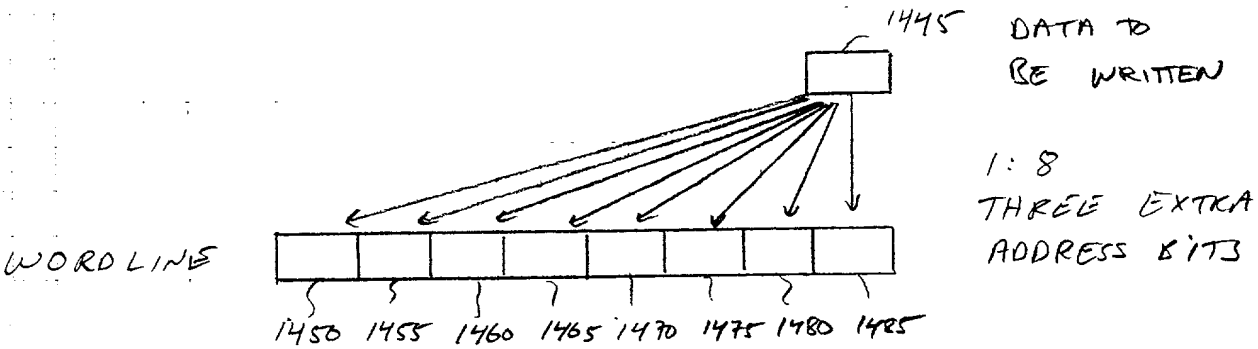


Figure 14C

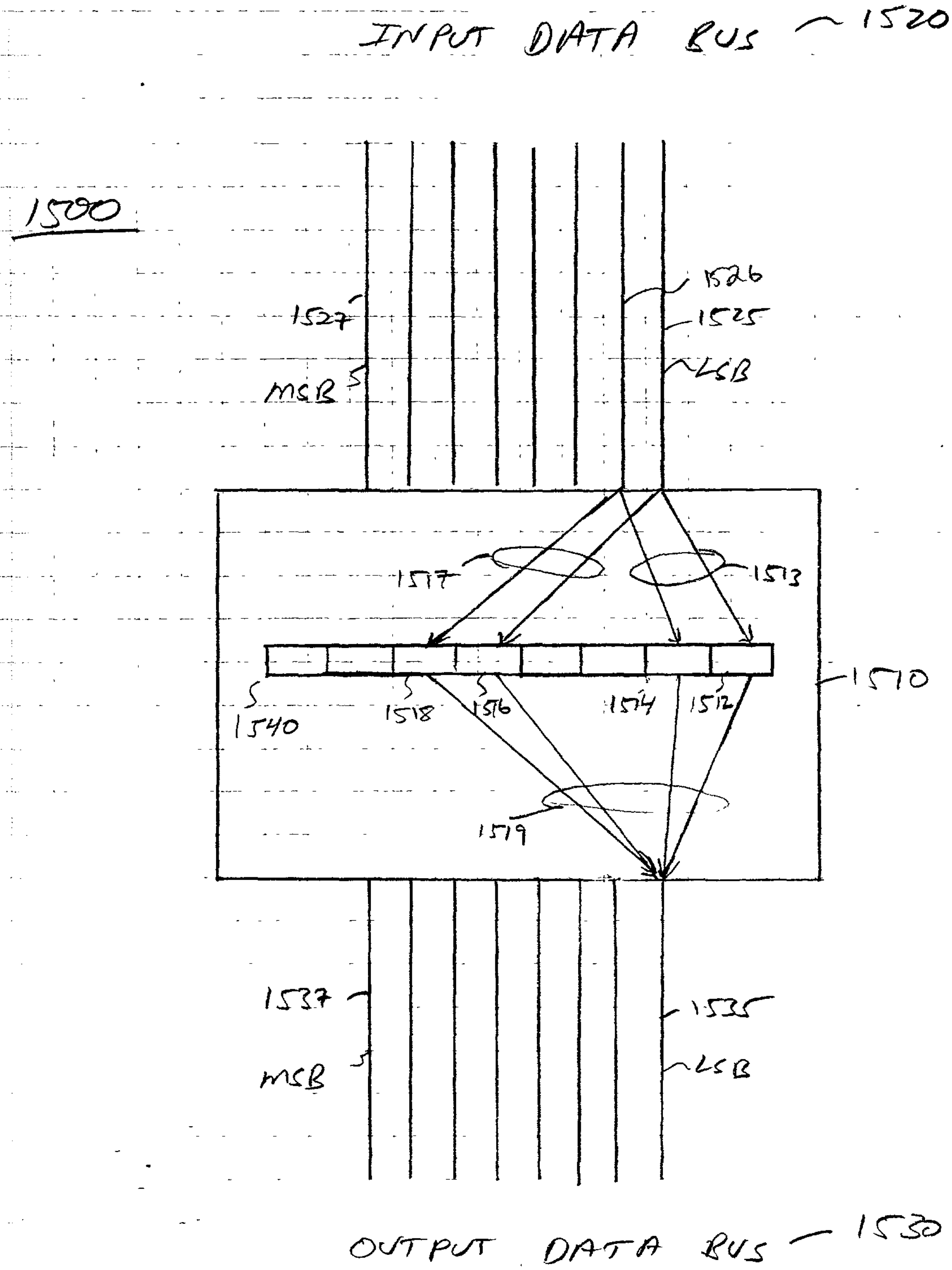

INPUT DATA BUS ~1520
1500
1526
1527
1525
MSB
LSB
1517
1513
1510
1540
1518
1516
1514
1512
1519
1537
1535
MSB
LSB
OUTPUT DATA BUS ~1530

FIGURE 15

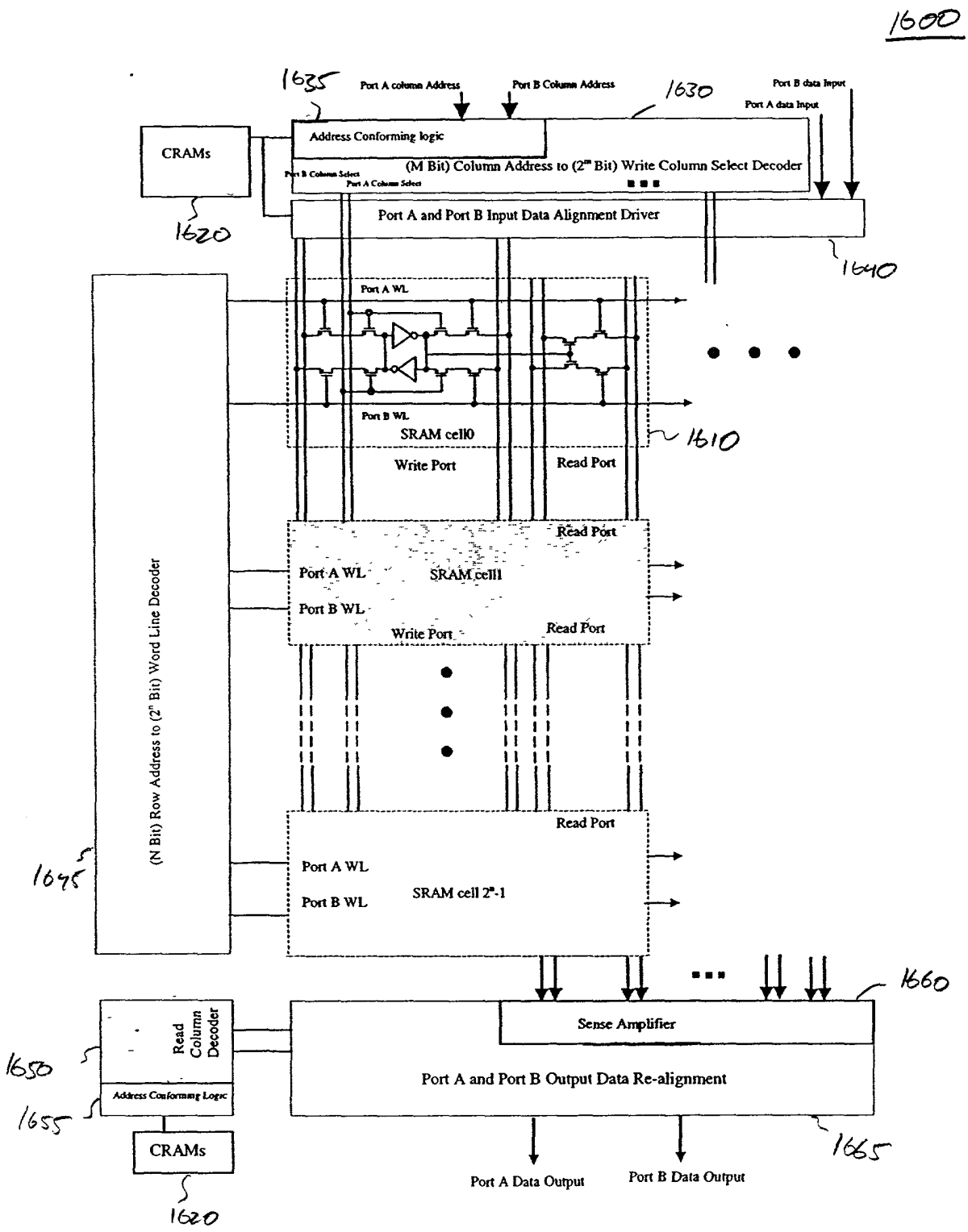

1600
1635
Port A column Address
Port B Column Address
1630
Port B data Input
Port A data Input
CRAMs
Address Conforming logic
(M Bit) Column Address to (2^m Bit) Write Column Select Decoder
Port B Column Select
Port A Column Select
Port A and Port B Input Data Alignment Driver
1620
1640
Port A WL
Port B WL
SRAM cell0
1610
Write Port
Read Port
Read Port
Port A WL
SRAM cell1
Port B WL
Write Port
Read Port
(N Bit) Row Address to (2^n Bit) Word Line Decoder
1645
Read Port
Port A WL
Port B WL
SRAM cell 2^n-1
1660
Sense Amplifier
Read Column Decoder
1650
Port A and Port B Output Data Re-alignment
Address Conforming Logic
1655
CRAMs
1620
1665
Port A Data Output
Port B Data Output

FIGURE 16

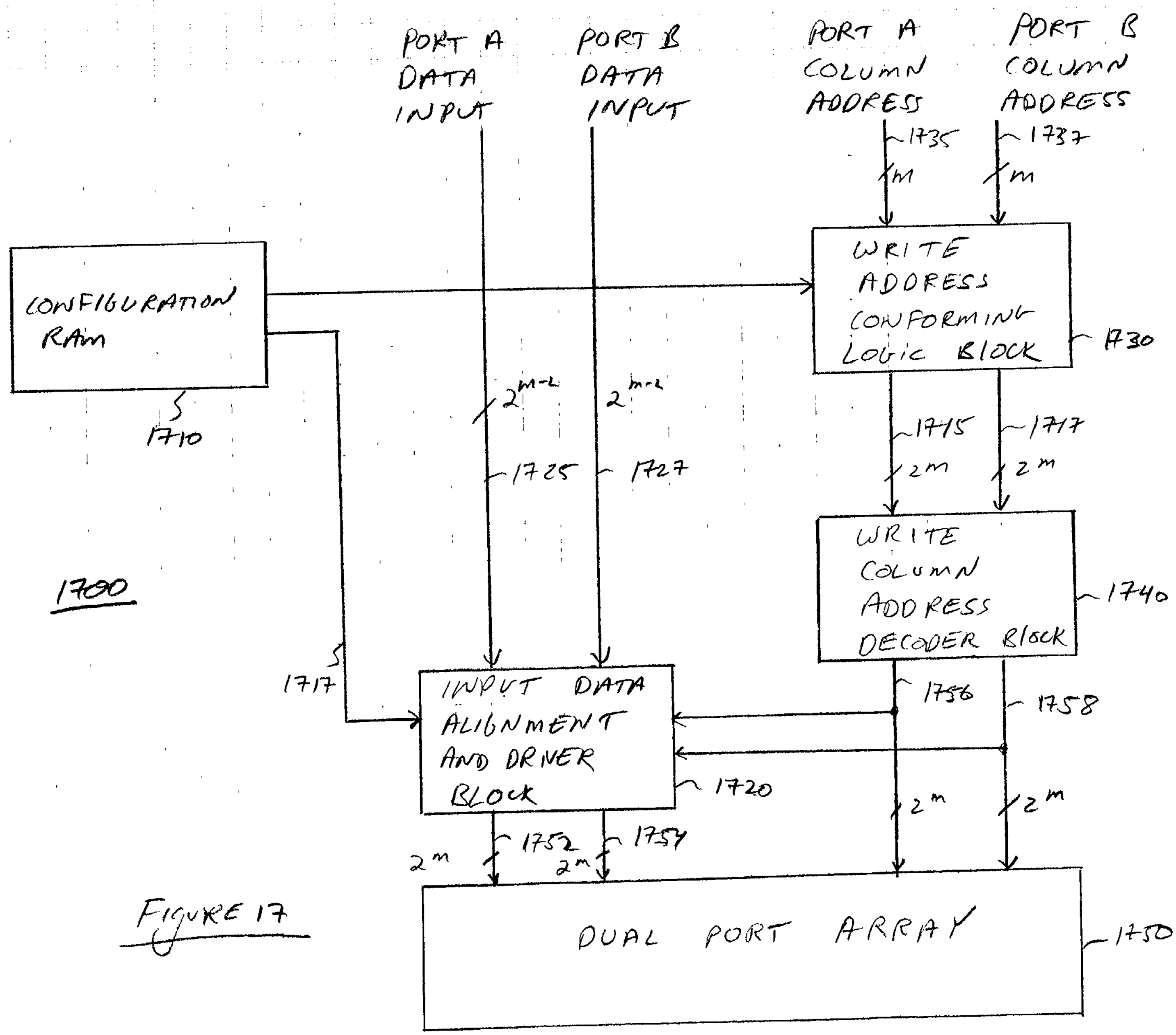

PORT A DATA INPUT
PORT B DATA INPUT
PORT A COLUMN ADDRESS
PORT B COLUMN ADDRESS
1735
1737
m
m
CONFIGURATION RAM
1710
WRITE ADDRESS CONFORMING LOGIC BLOCK
1730
2^{m-2}
2^{m-2}
1725
1727
1715
1717
2m
2^m
WRITE COLUMN ADDRESS DECODER BLOCK
1740
1700
1717
INPUT DATA ALIGNMENT AND DRIVER BLOCK
1720
1756
1758
2^m
2^m
1752
1754
2^m
2^m
DUAL PORT ARRAY
1750

FIGURE 17

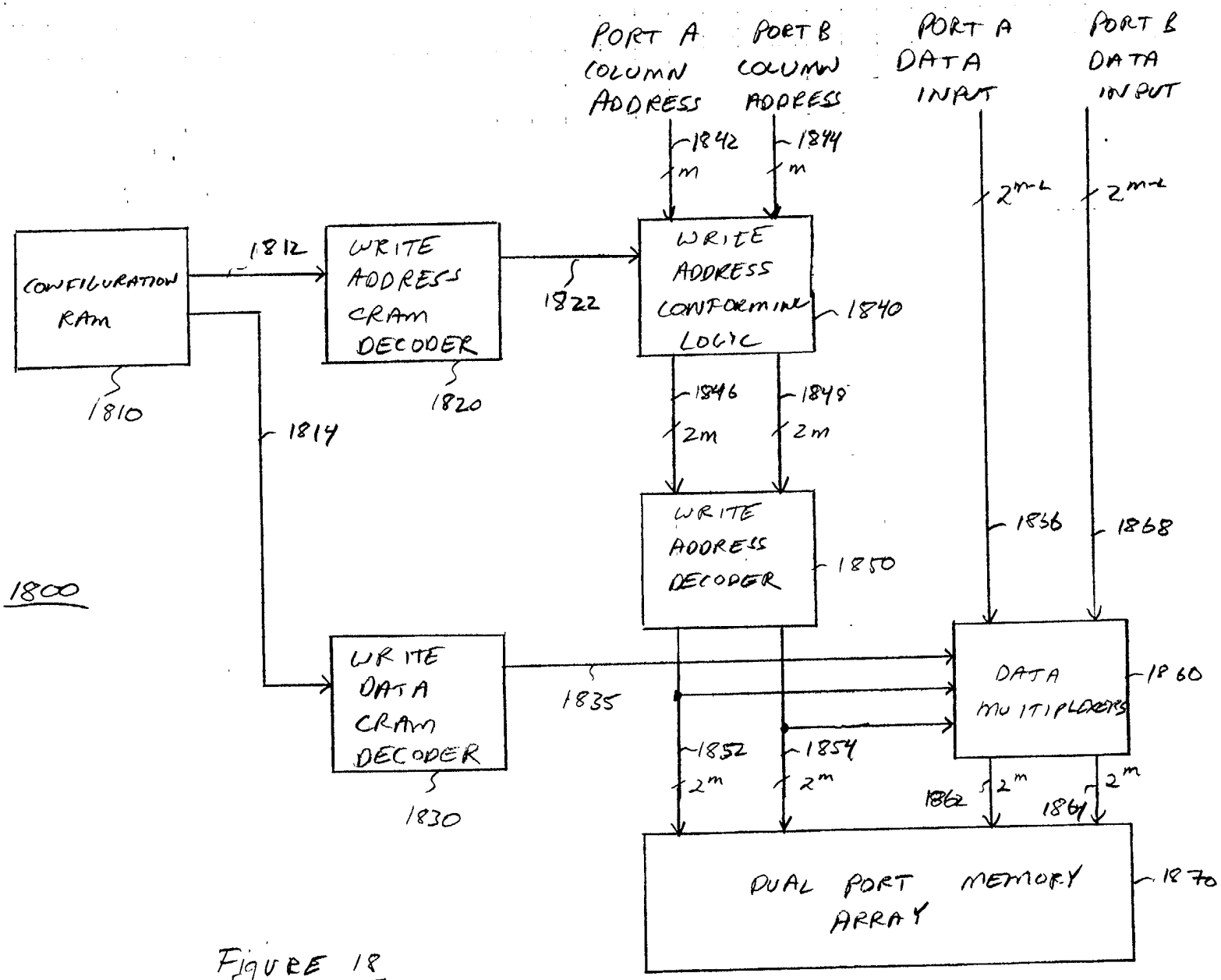


Figure 18

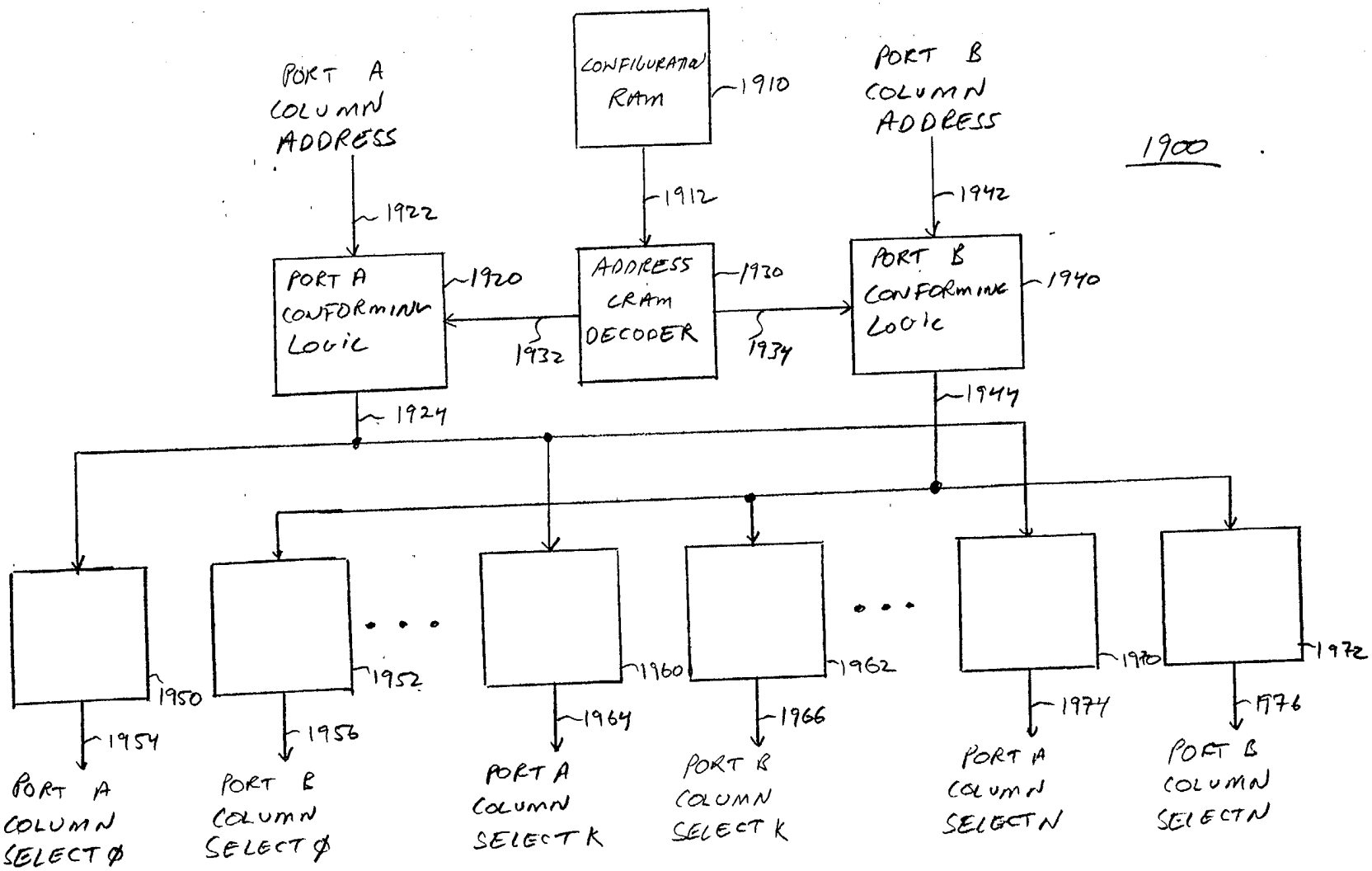

CONFIGURATION RAM
1910
PORT A COLUMN ADDRESS
1922
PORT B COLUMN ADDRESS
1942
1900
1912
PORT A CONFORMING LOGIC
1920
ADDRESS CRAM DECODER
1930
PORT B CONFORMING LOGIC
1940
1932
1934
1924
1944
1950
1952
1960
1962
1970
1972
1954
1956
1964
1966
1974
1976
PORT A COLUMN SELECT Ø
PORT B COLUMN SELECT Ø
PORT A COLUMN SELECT K
PORT B COLUMN SELECT K
PORT A COLUMN SELECT N
PORT B COLUMN SELECT N

Figure 19

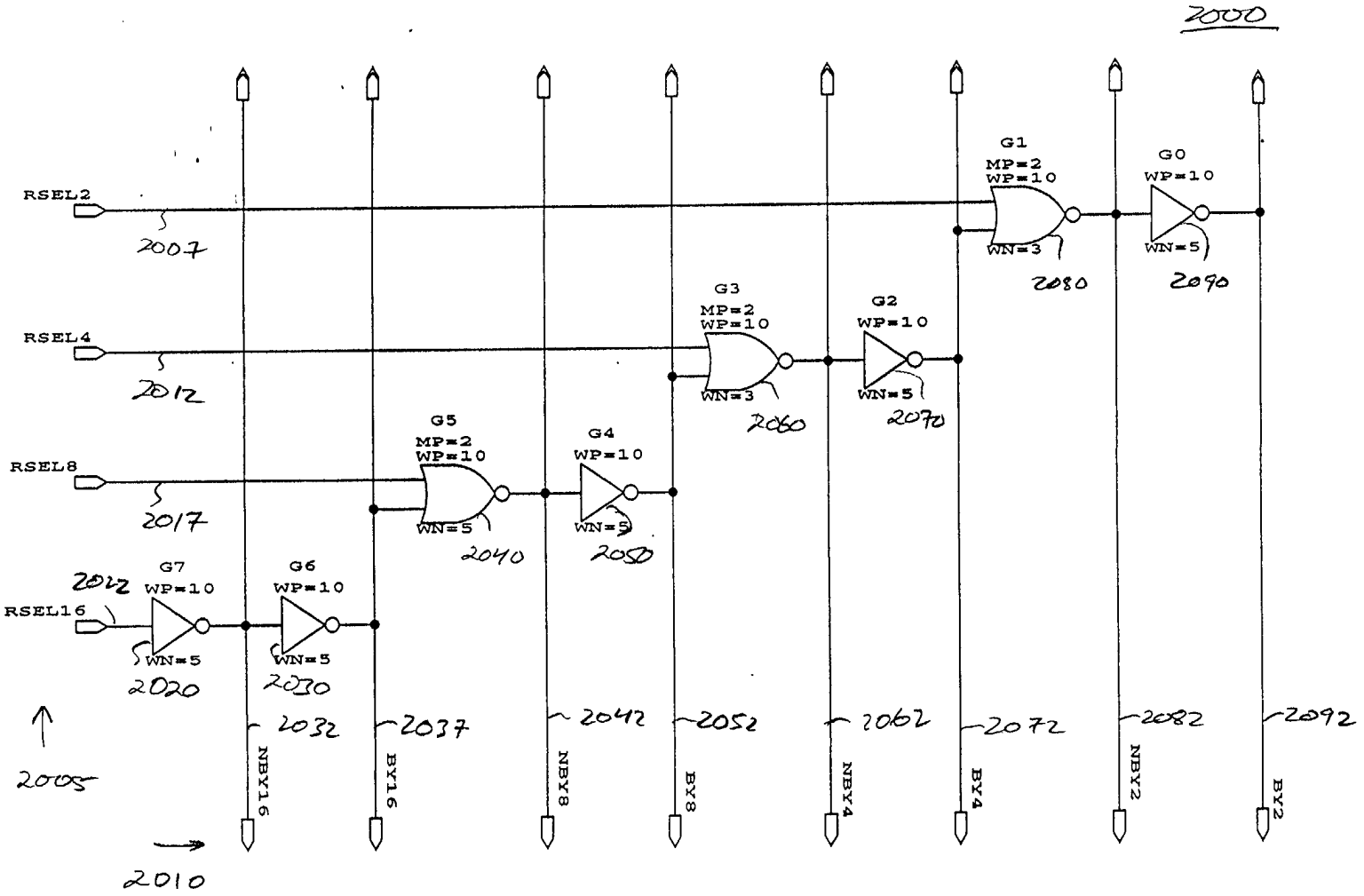

2000
RSEL2
2007
RSEL4
2012
RSEL8
2017
RSEL16
2022
G7
WP=10
WN=5
2020
G6
WP=10
WN=5
2030
G5
MP=2
WP=10
WN=5
2040
G4
WP=10
WN=5
2050
G3
MP=2
WP=10
WN=3
2060
G2
WP=10
WN=5
2070
G1
MP=2
WP=10
WN=3
2080
G0
WP=10
WN=5
2090
2005
2010
2032
2037
2042
2052
2062
2072
2082
2092
NBY16
BY16
NBY8
BY8
NBY4
BY4
NBY2
BY2

FIGURE 20

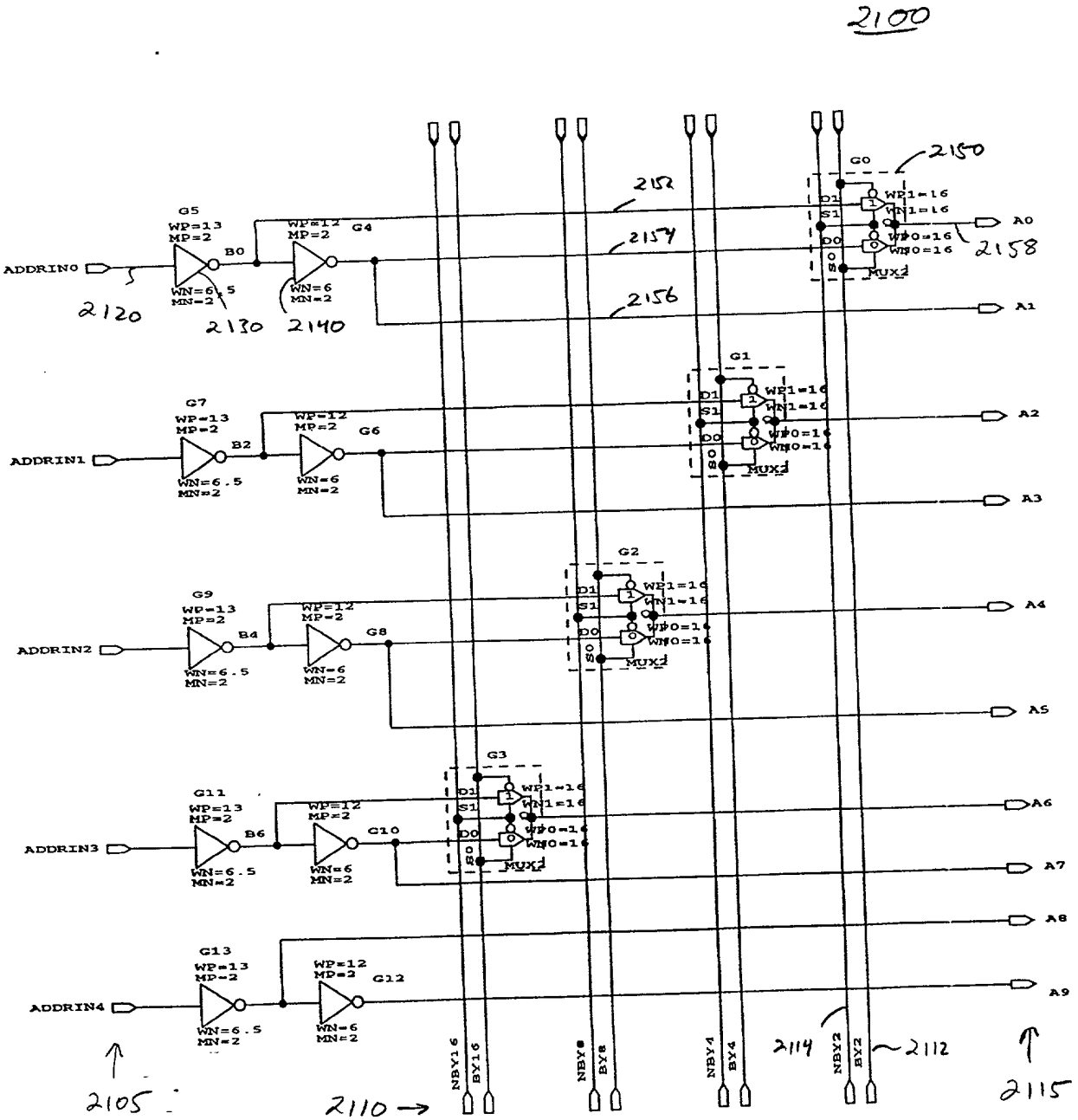
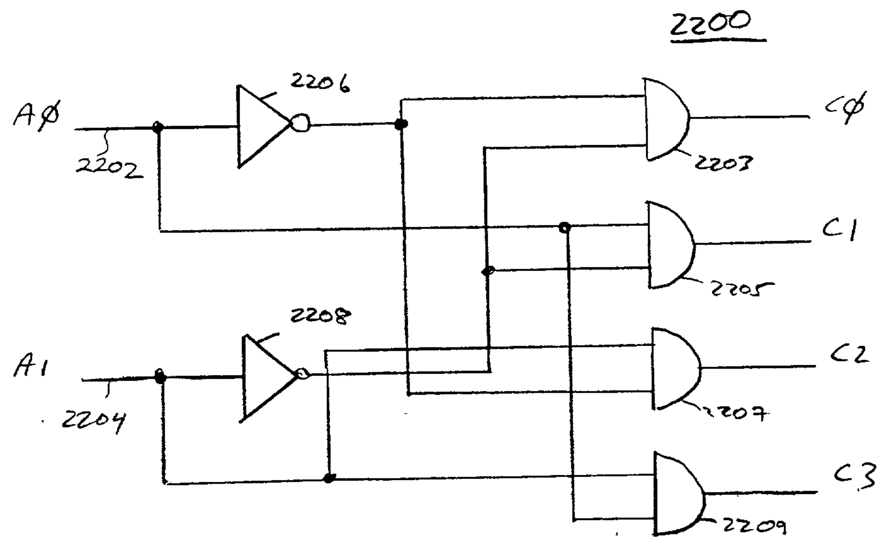

2100
G5
WP=13
MP=2
B0
WP=12
MP=2
G4
ADDRIN0
WN=6.5
MN=2
WN=6
MN=2
2120
2130
2140
2152
2154
2156
G0
2150
D1
S1
D0
S0
MUX2
WP1=16
WN1=16
WP0=16
WN0=16
A0
2158
A1
G7
WP=13
MP=2
B2
WP=12
MP=2
G6
ADDRIN1
WN=6.5
MN=2
WN=6
MN=2
G1
A2
A3
G9
WP=13
MP=2
B4
WP=12
MP=2
G8
ADDRIN2
WN=6.5
MN=2
WN=6
MN=2
G2
A4
A5
G11
WP=13
MP=2
B6
WP=12
MP=2
G10
ADDRIN3
WN=6.5
MN=2
WN=6
MN=2
G3
A6
A7
A8
G13
WP=13
MP=2
WP=12
MP=2
G12
ADDRIN4
WN=6.5
MN=2
WN=6
MN=2
A9
2105
2110
NBY16
BY16
NBY8
BY8
NBY4
BY4
NBY2
BY2
2114
2112
2115

Figure 21

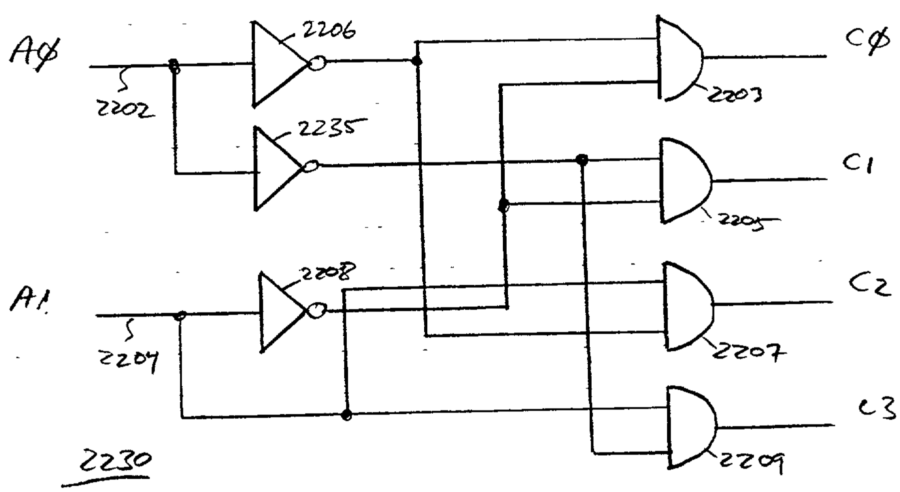


2210

A1	AØ	CØ	C1	C2	C3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

2220

$$C\phi = \overline{A1} \cdot \overline{A\phi}$$
$$C1 = \overline{A1} \cdot A\phi$$
$$C2 = A1 \cdot \overline{A\phi}$$
$$C3 = A1 \cdot A\phi$$



2240

$$C\phi = \overline{A1} \cdot \overline{A\phi}$$
$$C1 = \overline{A1} \cdot \overline{A\phi}$$
$$C2 = A1 \cdot \overline{A\phi}$$
$$C3 = A1 \cdot \overline{A\phi}$$

2250

A1	AØ	CØ	C1	C2	C3	
0	0	1	1	0	0	~2252
0	1	0	0	0	0	-2254
1	0	0	0	1	1	-2256
1	1	0	0	0	0	-2258

FIGURE 22

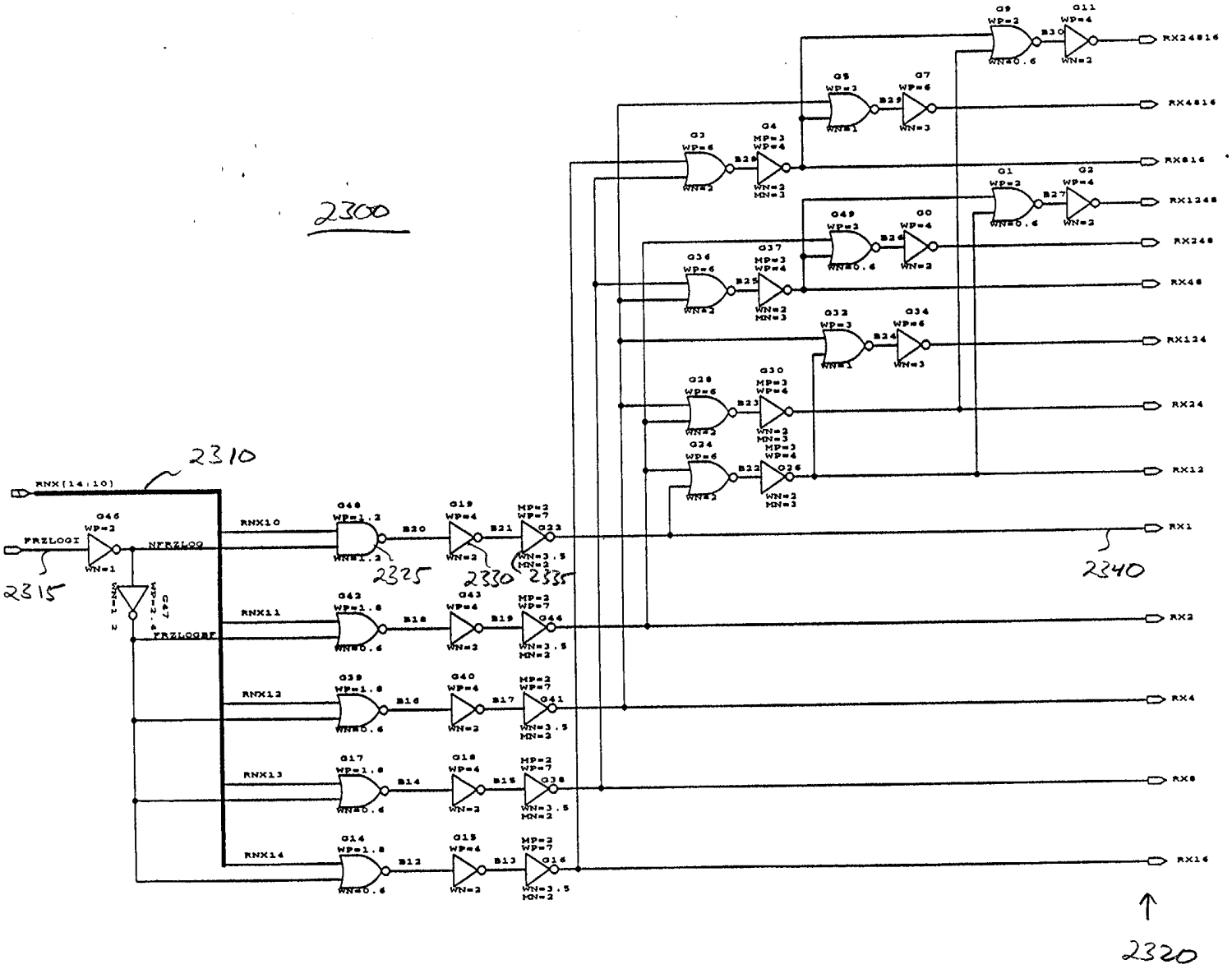
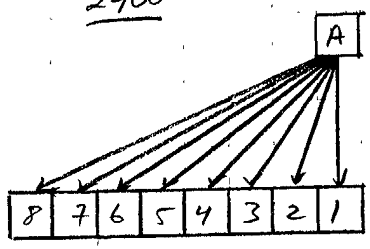
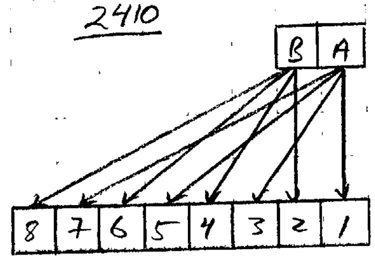


FIGURE 23

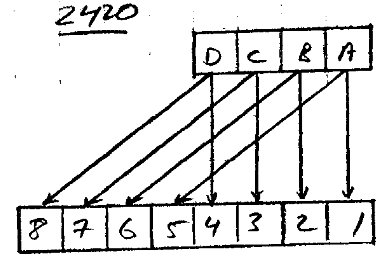
2400



2410



2420



2430

MUX (2432)	# bits/word (2434): 1	2	4	INPUTS (2436)	TYPE MUX (2438)
1	A	A	A	A	1:1
2	A	B	B	A, B	2:1
3	A	A	C	A, C	2:1
4	A	B	D	A, B, D	3:1
5	A	A	A	A	1:1
6	A	B	B	A, B	2:1
7	A	A	C	A, C	2:1
8	A	B	D	A, B, D	3:1

2440

MUX (2442)	OUTPUTS (2444)	TYPE MUX (2446)
A	8, 7, 6, 5, 4, 3, 2, 1	1:8
B	8, 6, 4, 2	1:4
C	7, 3	1:2
D	8	1:1

FIGURE 24

2500

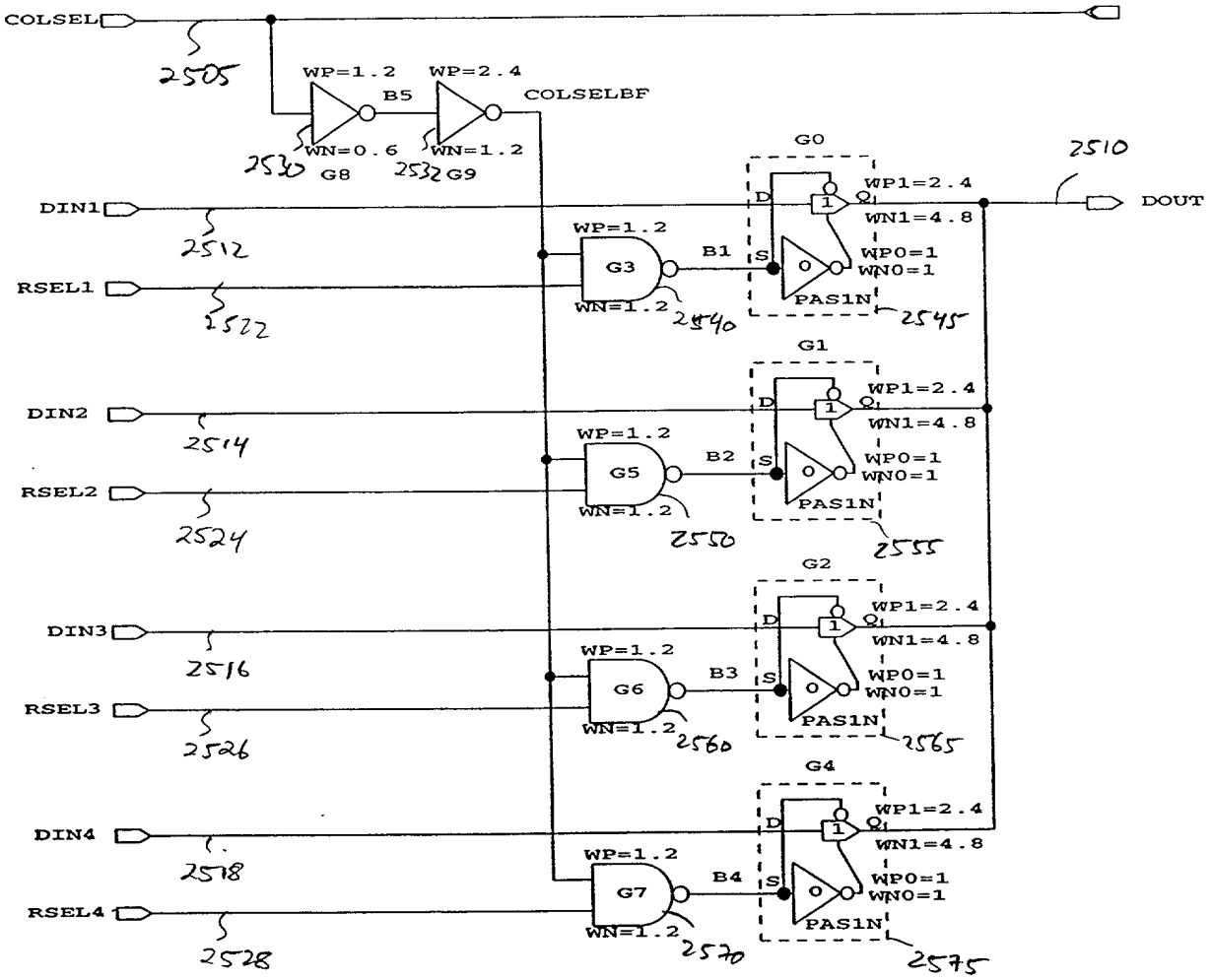


FIGURE 25

2600

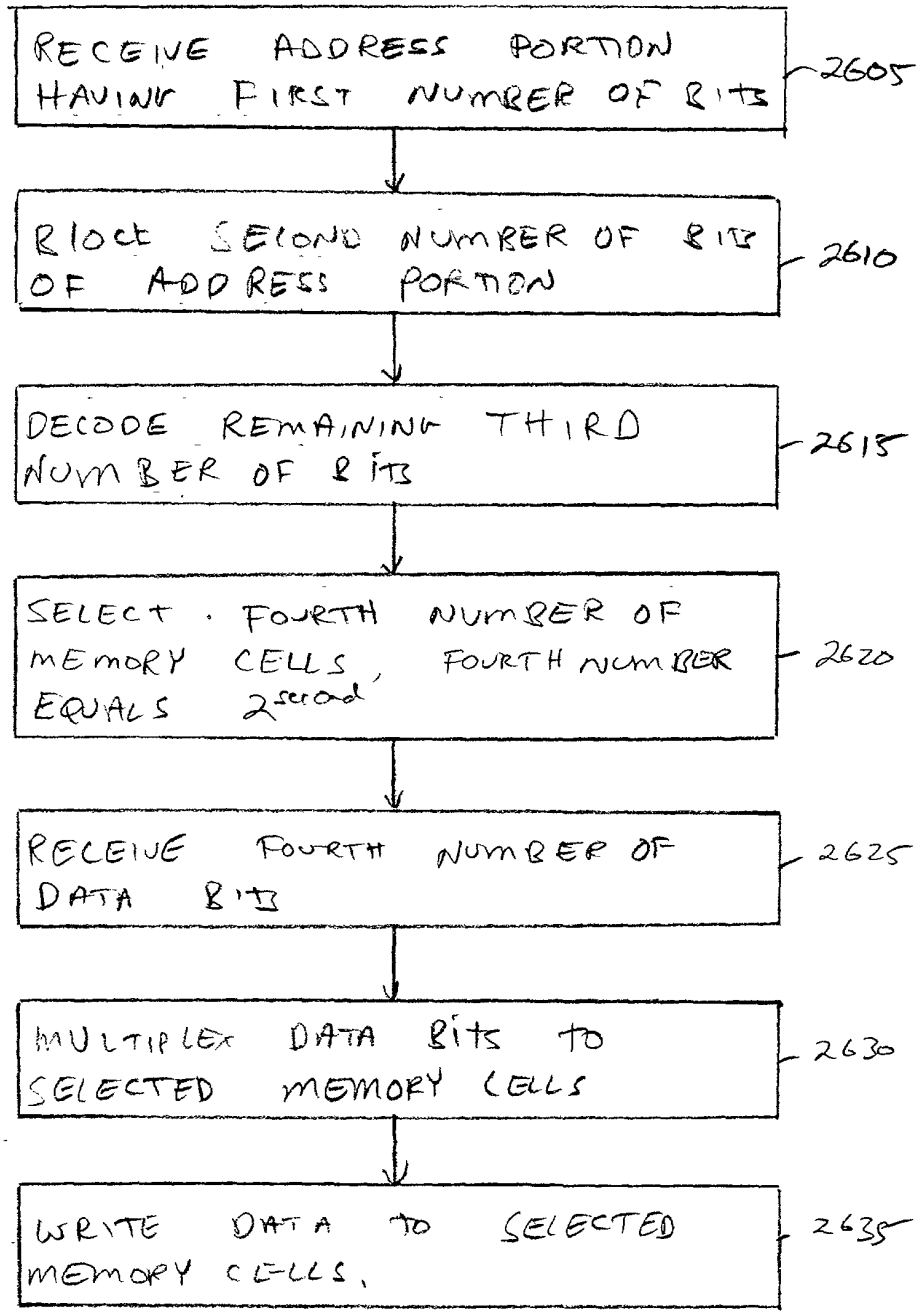


FIGURE 26

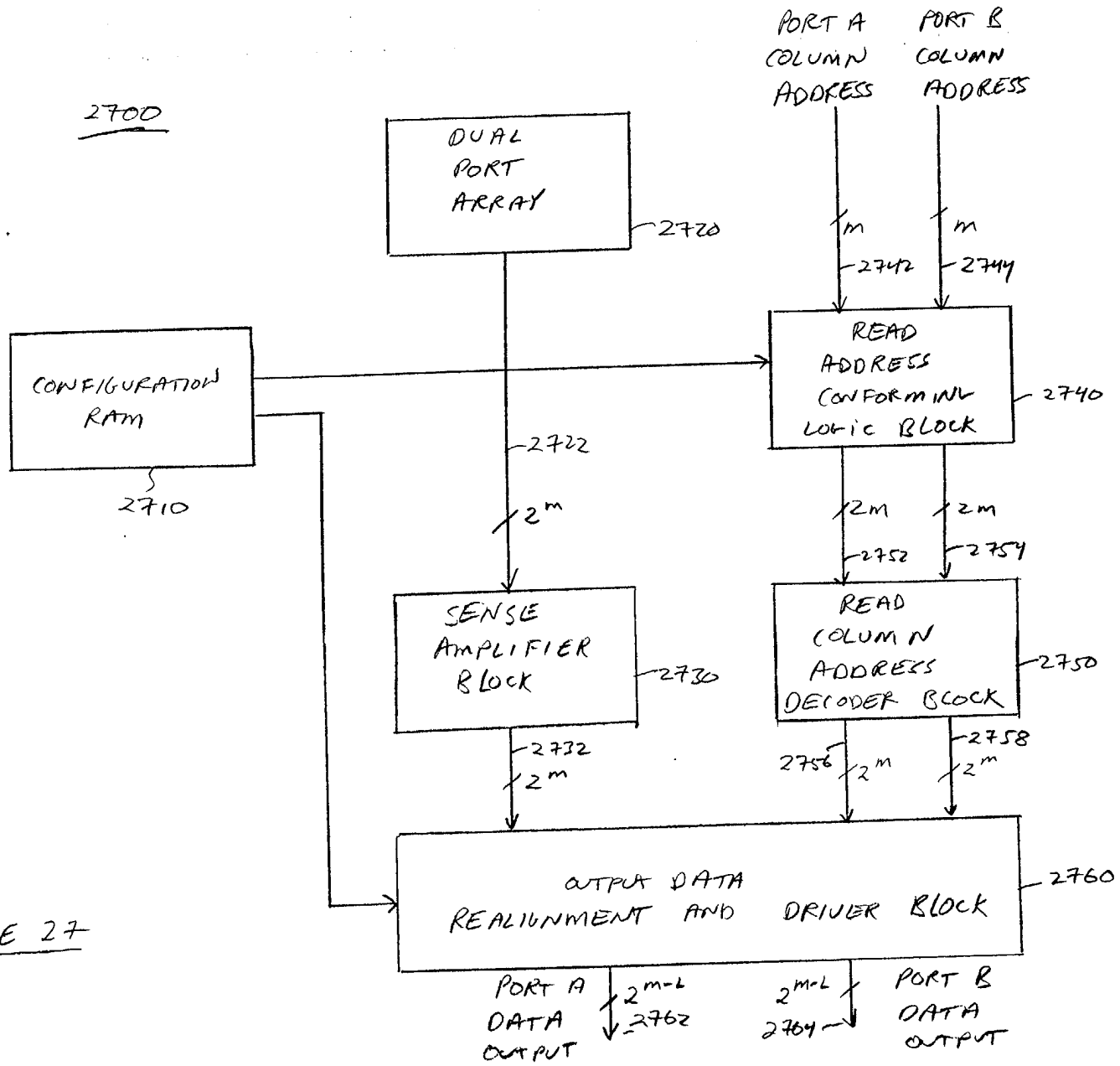


Figure 27

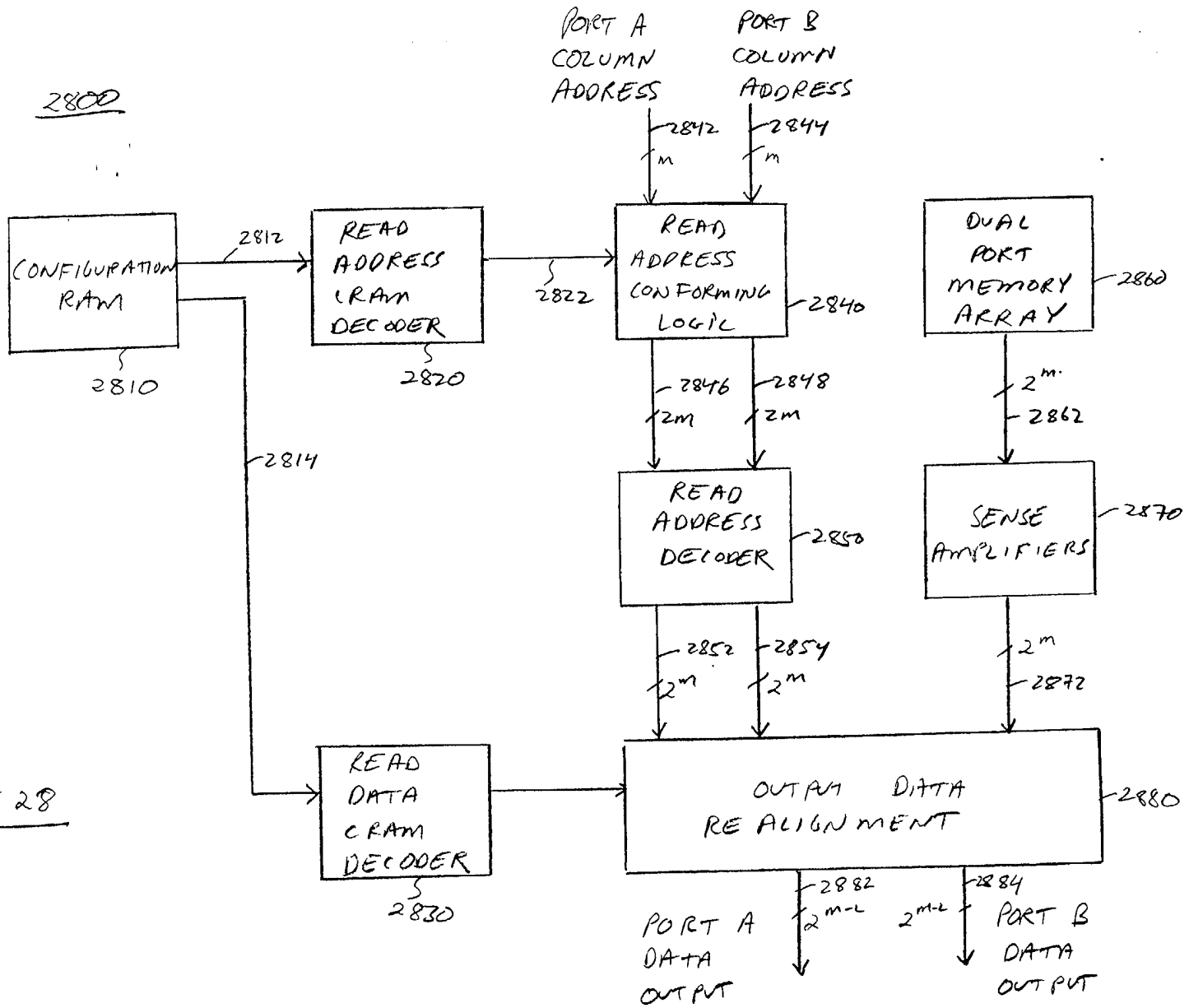
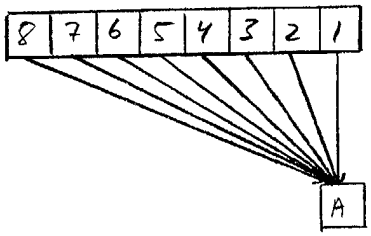
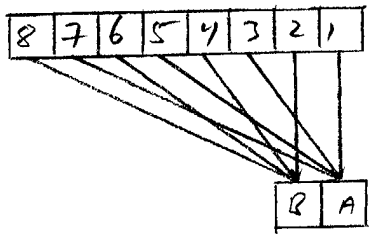


Figure 28

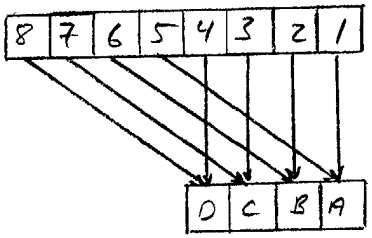
2900



2910



2920



2930

MUX (2932)	#bits/word (2934): 1	2	4	OUTPUTS (2936)	TYPE MUX (2938)
1	A	A	A	A	1:1
2	A	B	B	A, B	1:2
3	A	A	C	A, C	1:2
4	A	B	D	A, B, D	1:3
5	A	A	A	A	1:1
6	A	B	B	A, B	1:2
7	A	A	C	A, C	1:2
8	A	B	D	A, B, D	1:3

2940

MUX (2942)	INPUTS (2944)	TYPE MUX (2946)
A	8, 7, 6, 5, 4, 3, 2, 1	8:1
B	8, 6, 4, 2	4:1
C	7, 3	2:1
D	8	1:1

FIGURE 29

3000

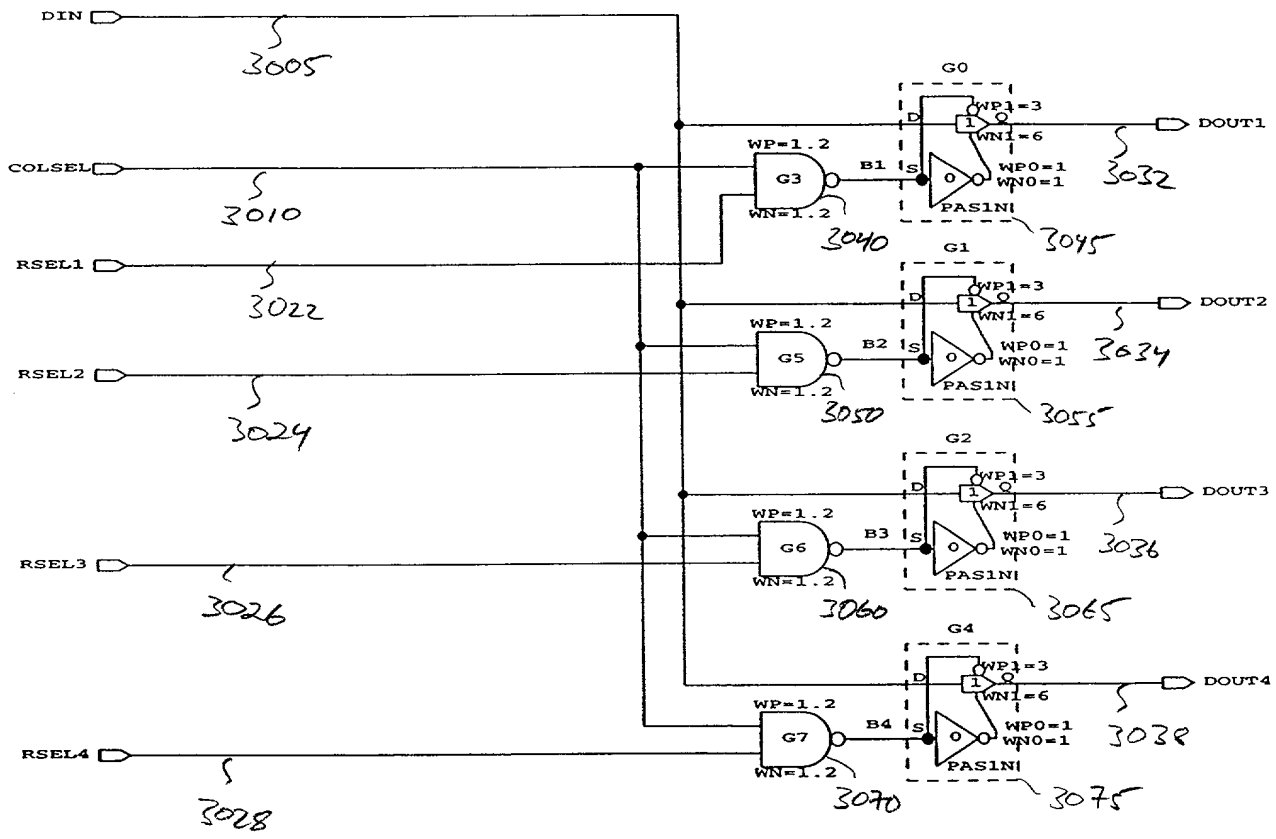


FIGURE 30

3100

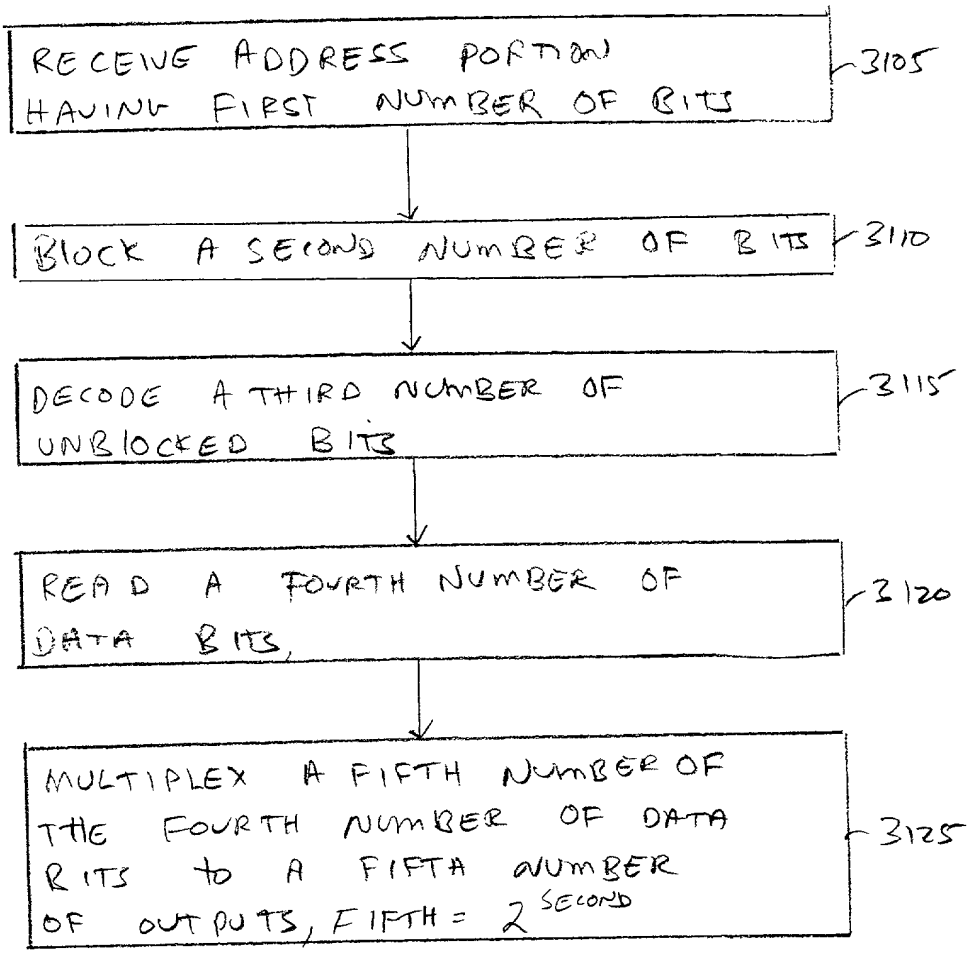


Figure 31